NOTES:

1. Project Drawing Numbers:

Raw PCB	100-0330631-A1
Gerber Files	110-0330631-A1
PCB Design Files	120-0330631-A1
Assembly Drawing	130-0330631-A1
Fab Drawing	140-0330631-A1
Schematic Drawing	150-0330631-A1
PCB Film	160-0330631-A1
Bill of Materials	170-0330631-A1
Schematic Design Files	180-0330631-A1
Functional Specification	210-0330631-A1
PCB Layout Guidelines	220-0330631-A1
Assembly Rework	320-0330631-A1

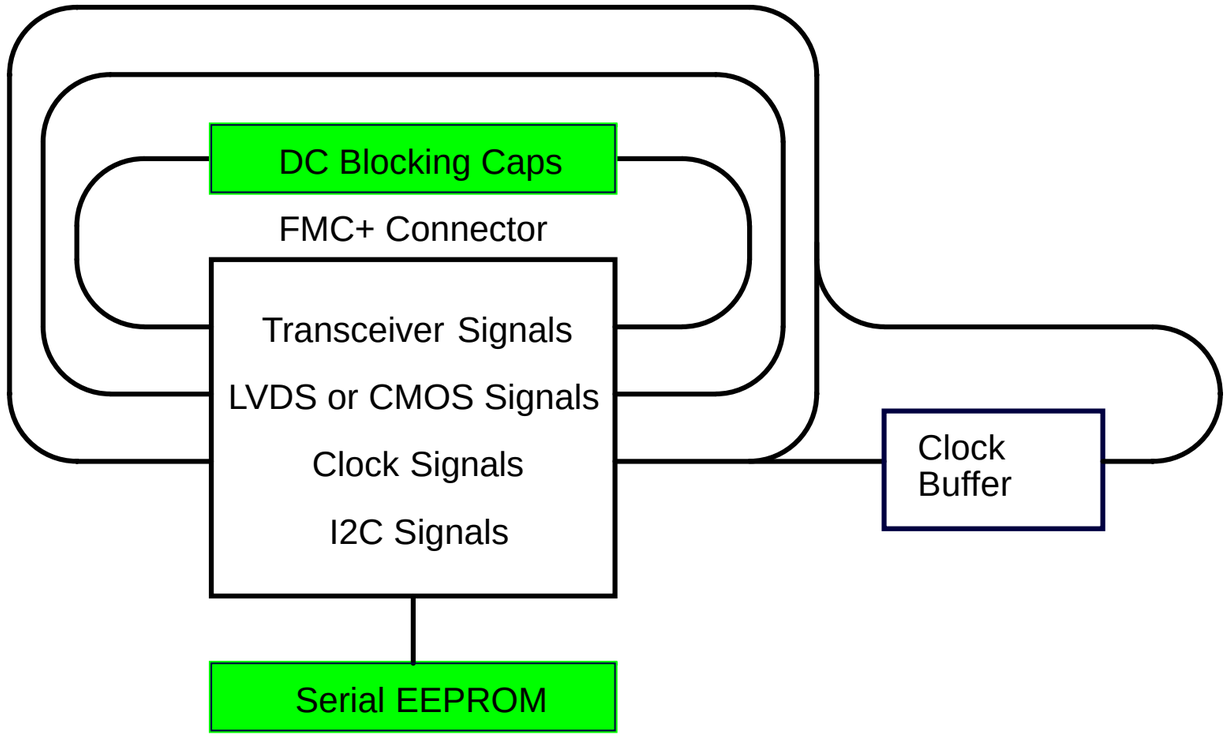
2. The FMC+ pinout was based on v57d4-r1d0t-2016-Mar-17, table 5-1.
3. This board was designd for Stratix 10 SI Development kit rev A.

Pre-Release Schematic
DO NOT COPY

REV	DATE	PAGES	DESCRIPTION
01	07/22/16	All	Preliminary

PAGE	DESCRIPTION
1	Title, Notes, Block Diagram, Rev. History
2	FMC+ LA / HA / HB
3	FMC+ DP
4	Clock Buffer

FMC+ Loopback



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Title: **FMC+ Loopback Card**

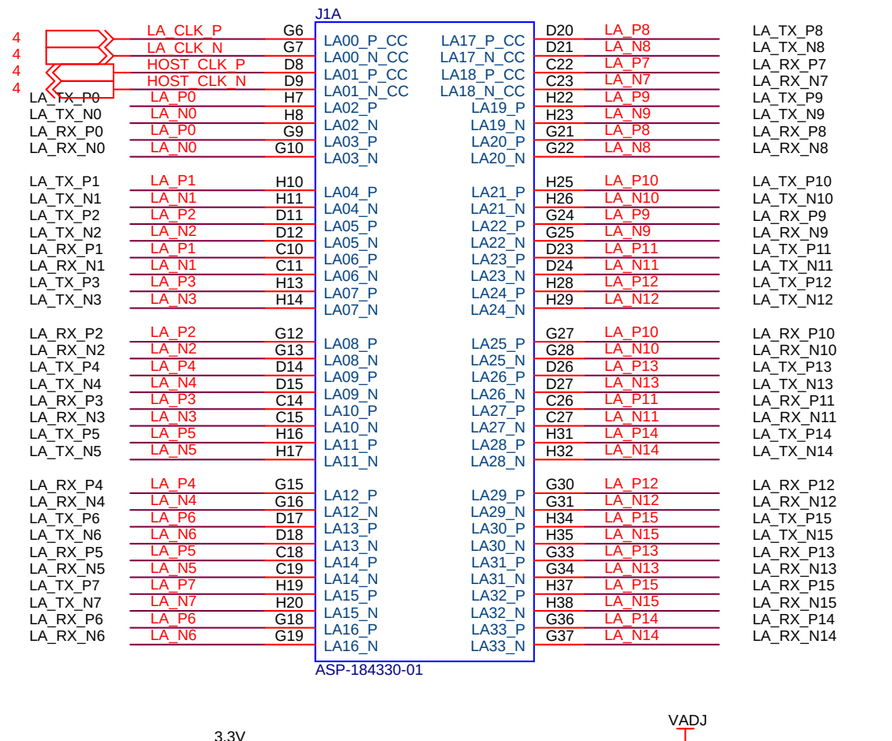
Size	Document Number	Rev
B	150-0330631-A1 (6XX-44455R)	A1

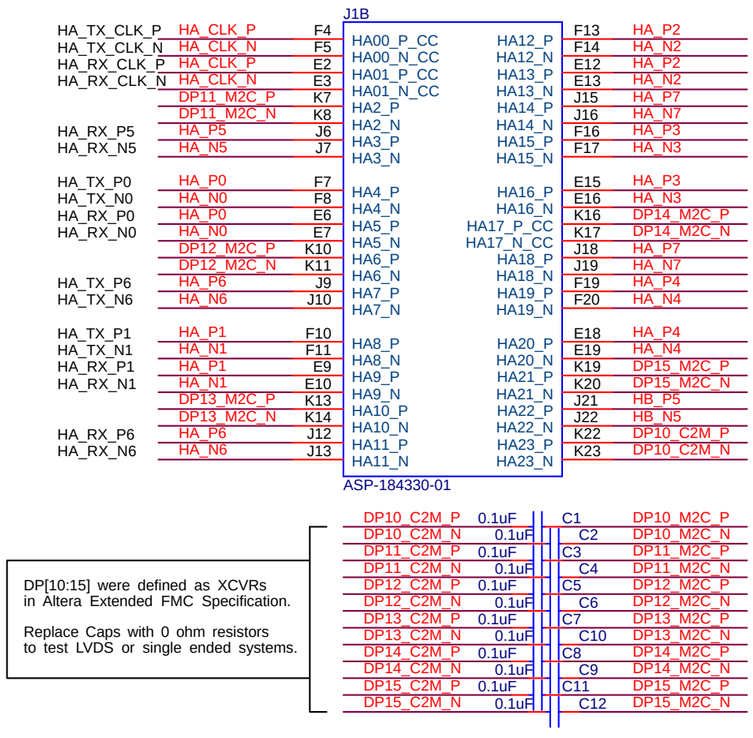
Date: Tuesday, August 23, 2016 Sheet 1 of 4

FMC+ LA / HA / HB

LA[33:0]/HA[23:0]/HB[21:0] loopback are following the Altera Extended FMC Specification, which are backward compatible with FMC loopback card pinout.

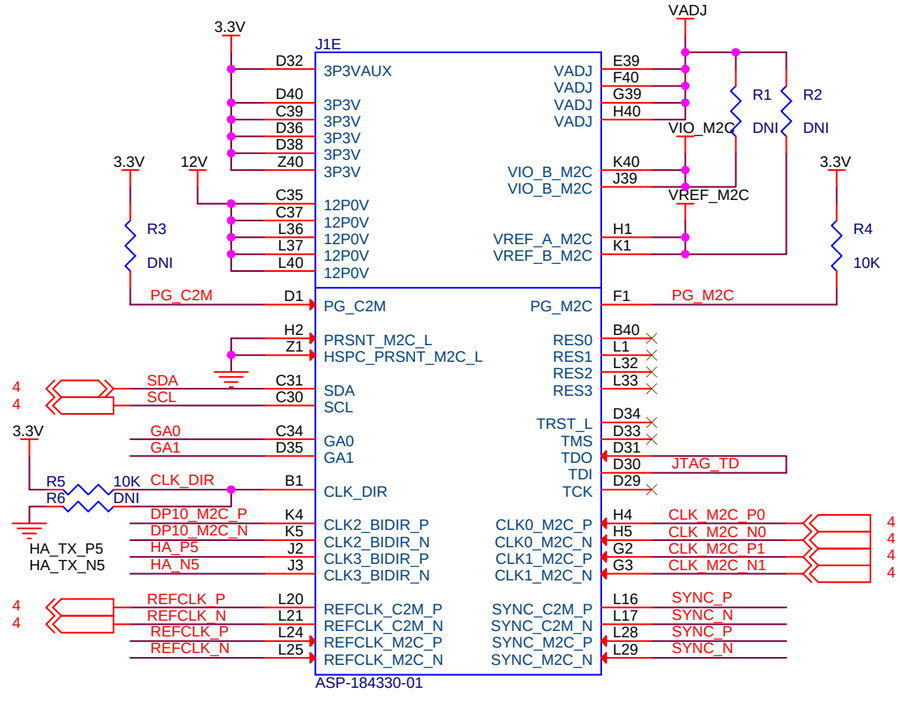
TX/RX direction are shown in text aside.

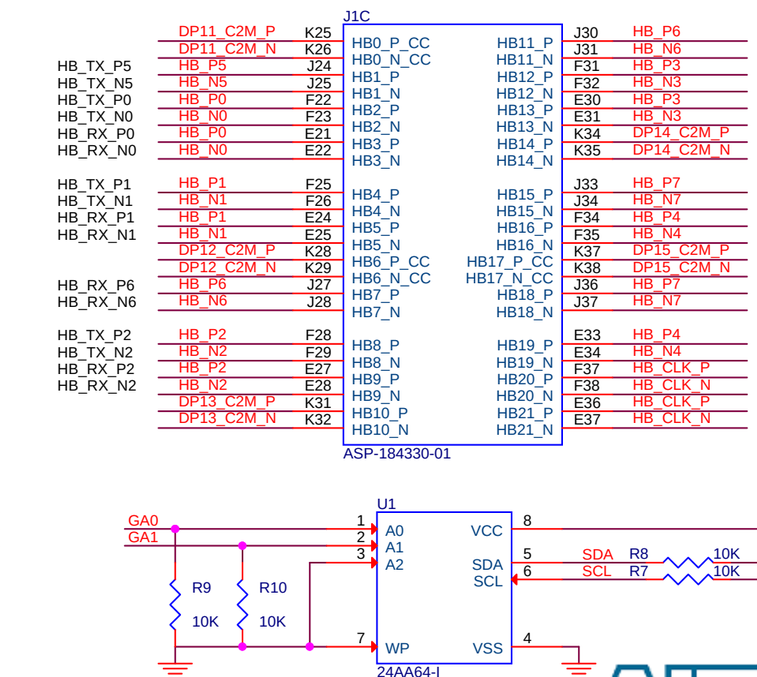


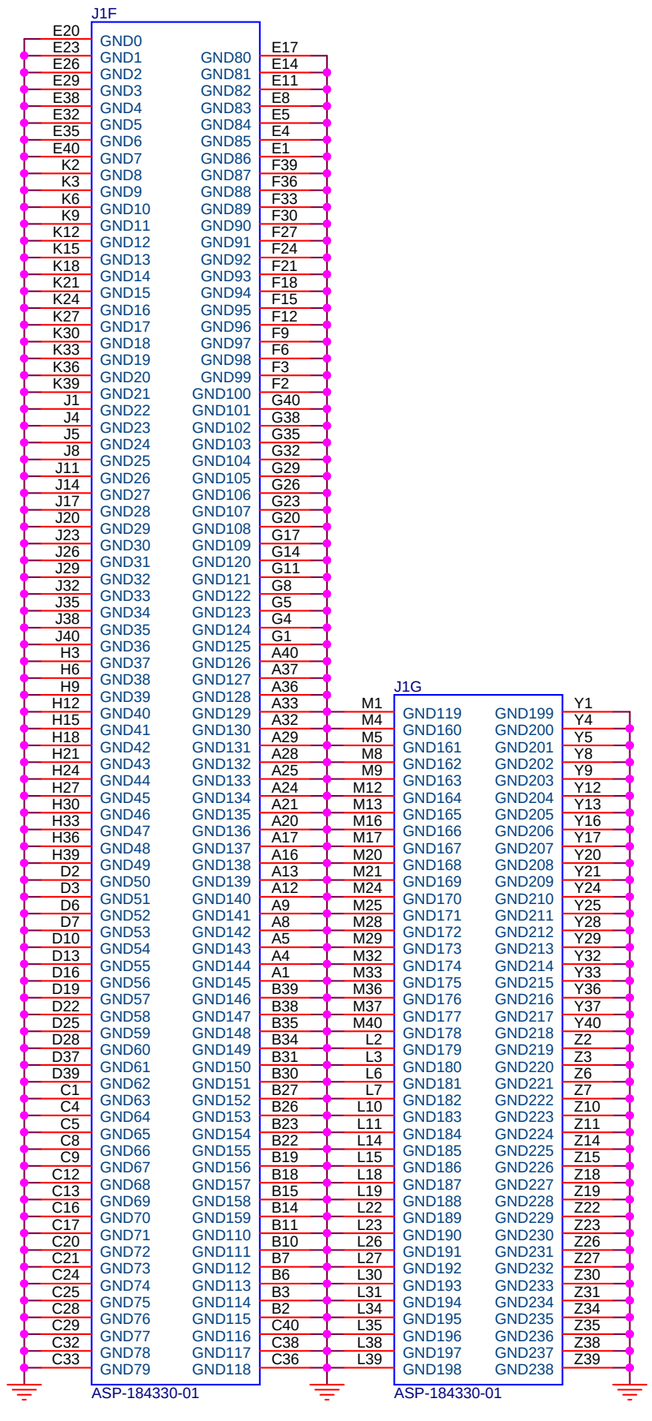


DP[10:15] were defined as XCVRs in Altera Extended FMC Specification.

Replace Caps with 0 ohm resistors to test LVDS or single ended systems.



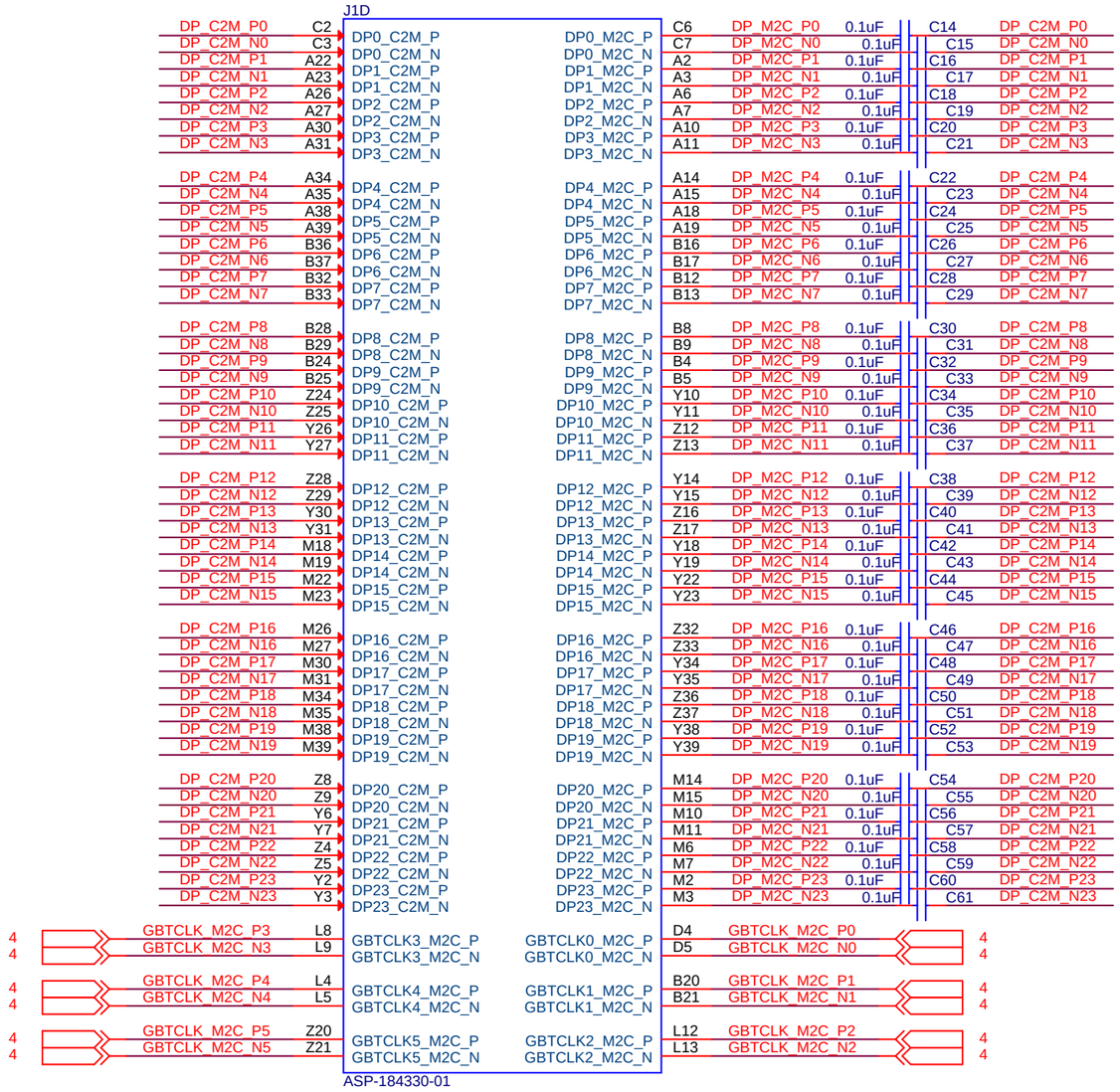




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Title	FMC+ Loopback Card	
Size B	Document Number 150-0330631-A1 (6XX-44455R)	Rev A1
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FMC+ DP



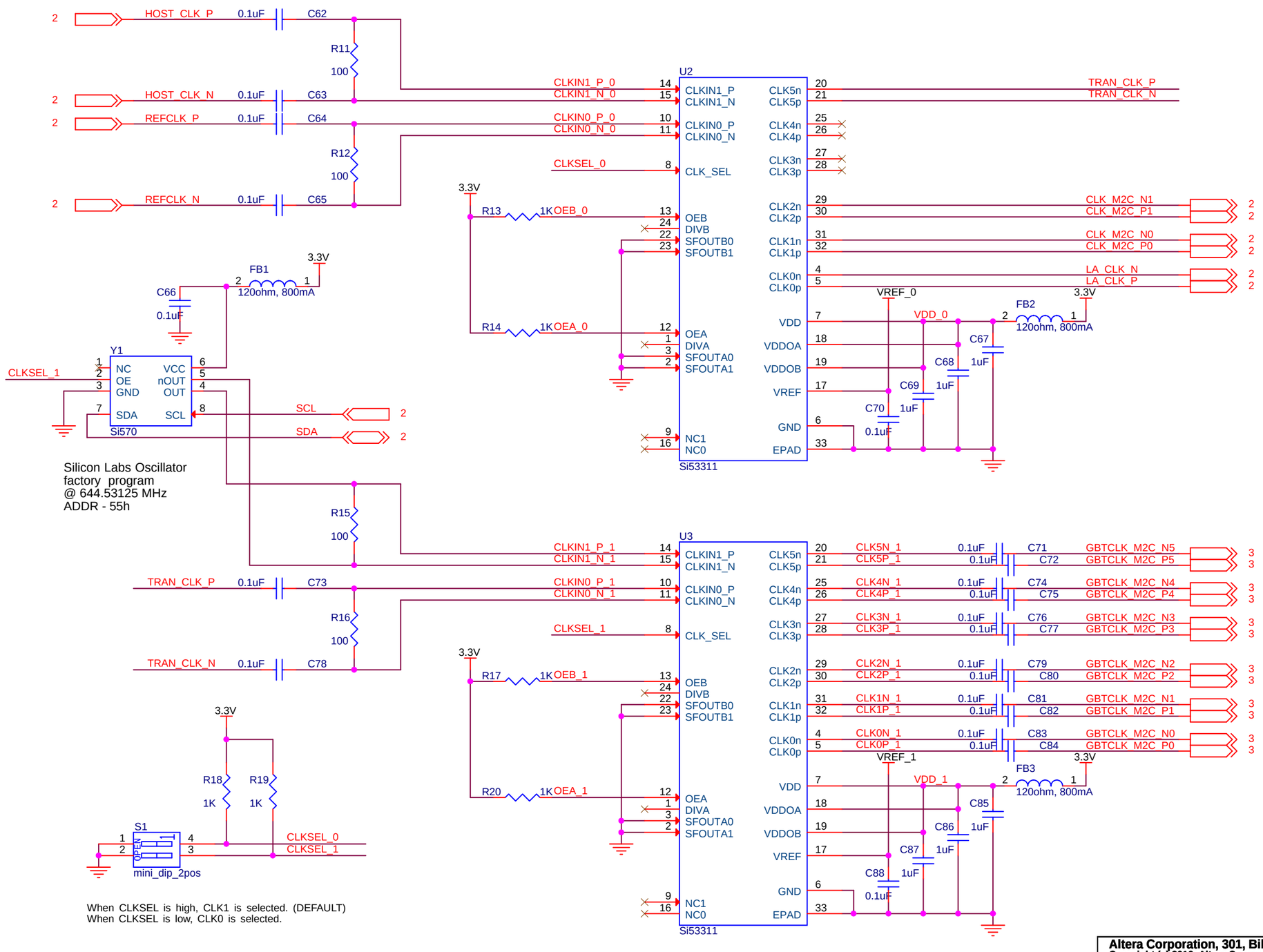
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Title: **FMC+ Loopback Card**

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Clock Buffer



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