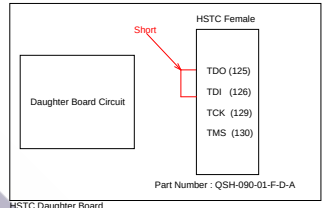
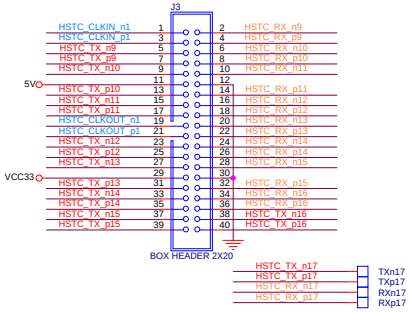
Attention:

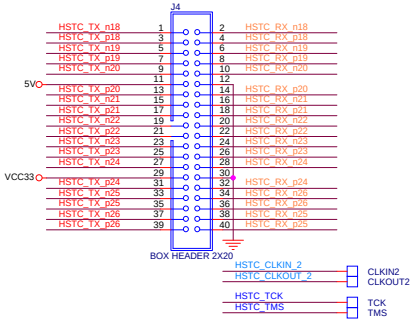
1. Both JTAG and I2C signals are fixed at 3.3V.
2. If the JTAG signals are not used on the daughter board, please short TDI with TDO (see Example 2).
3. The voltage level of VTT and VREF is half the I/O voltage of the HSTC connector.
4. Daughter board should supply power to VTT and VREF.
5. Pin 2 must be connected to GND to enable the auto JTAG chain detection.

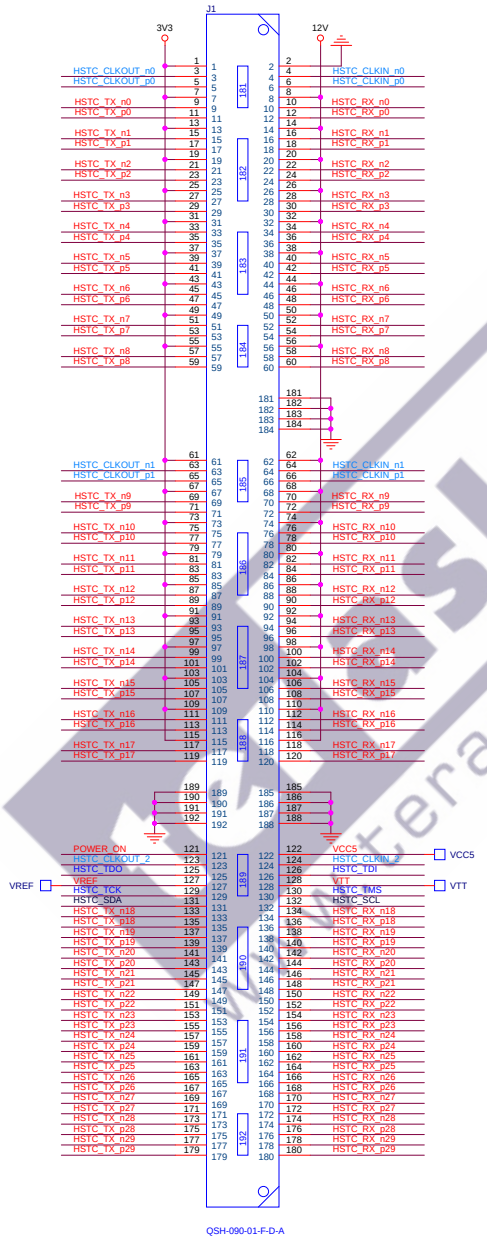
Example 2:



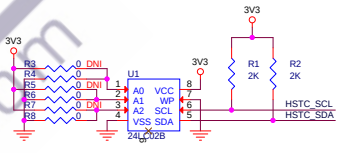
HSTC Daughter Board

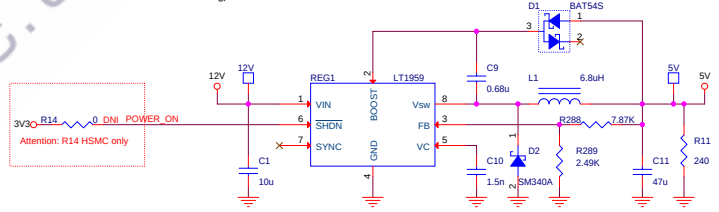


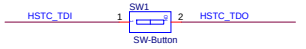


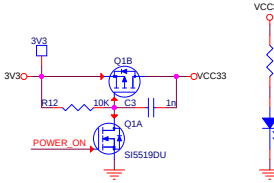


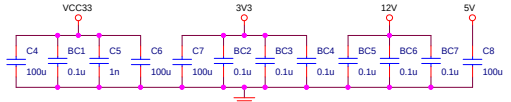
HSTC Connector - Female (Motherboard Bottom-side)
or Daughter Board











Title: HSTC TO GPIO Daughter Board

Size	Document Number	Rev
C	High Speed Terasic Connector (HSTC)	B

Date: Thursday, April 03, 2014 Sheet 1 of 1