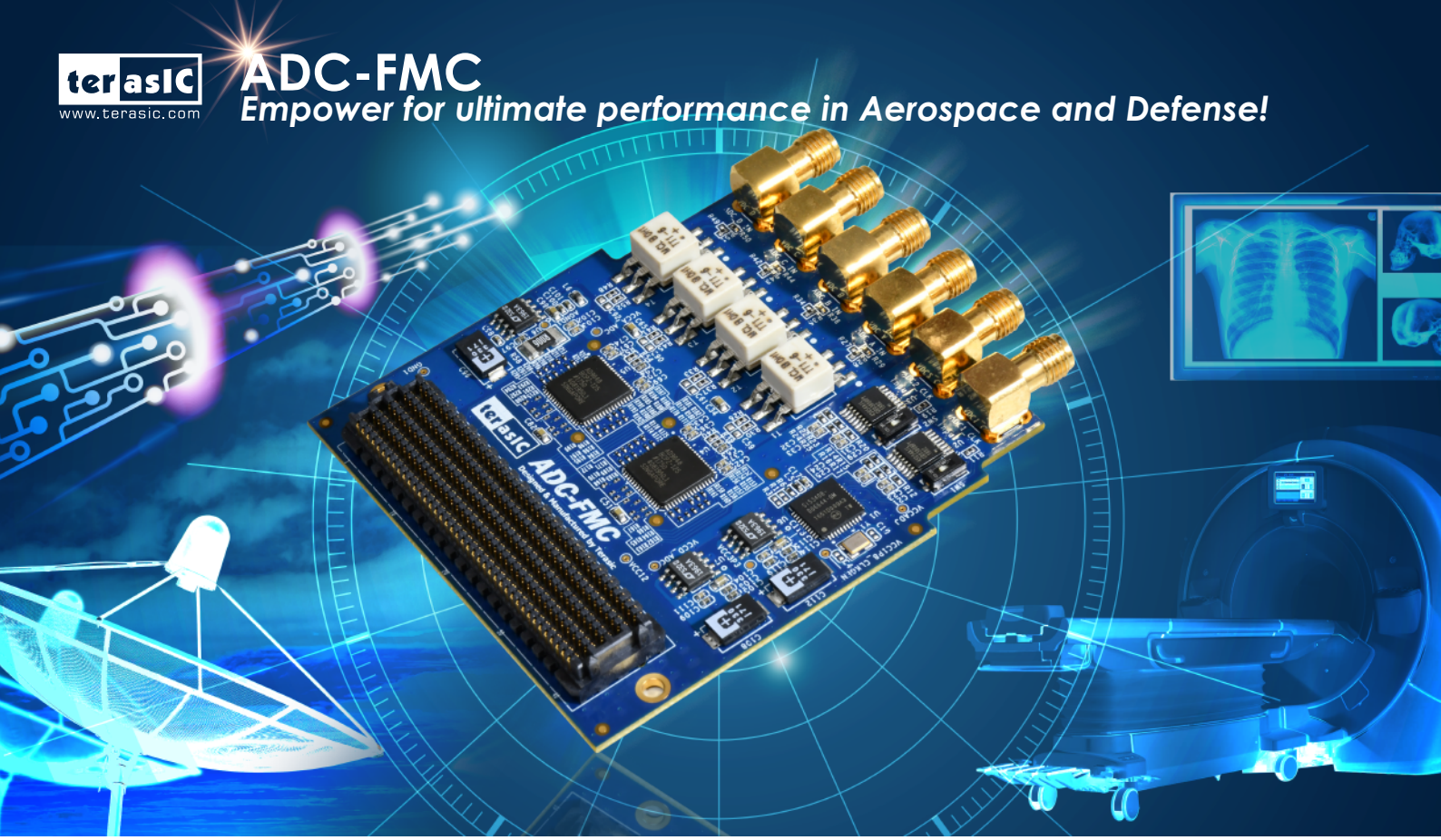
ADC-FMC

Empower for ultimate performance in Aerospace and Defense!



Introduction

Terasic's ADC-FMC board is a four-channel high-speed ADC daughter card. The board is designed with the goal to develop advanced Aerospace and Defense systems that achieve the highest levels of performance while reducing size, weight, power, system cost and development time.

The board is equipped with two *AD9648BCPZ-125* chips - one AD9648BCPZ-125 chip can provide two ADC channels, and each channel can provide maximal 125 MSPS with 14-bits resolution data. The ADC contains several features designed to maximize flexibility and minimize system cost, such as programmable clock and data alignment and programmable digital test pattern generation. Plus, the build-in onboard clock generator (si5340B) provides the reference clock for the ADC chip. The reference clock can also come fro FPGA main board; or route the clock source externally through the onboard SMA connectors.

Overall, the ADC-FMC provides best-in-class bandwidth, power and dynamic range to help developers achieve excellent ADC performance in a variety of applications and critical environments.

Target Applications

- Aerospace and Defense
- Radar/Lidar
- Broadband Data Applications
- Communications
- Medical Imaging
- Diversity Radio Systems

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Customized Services

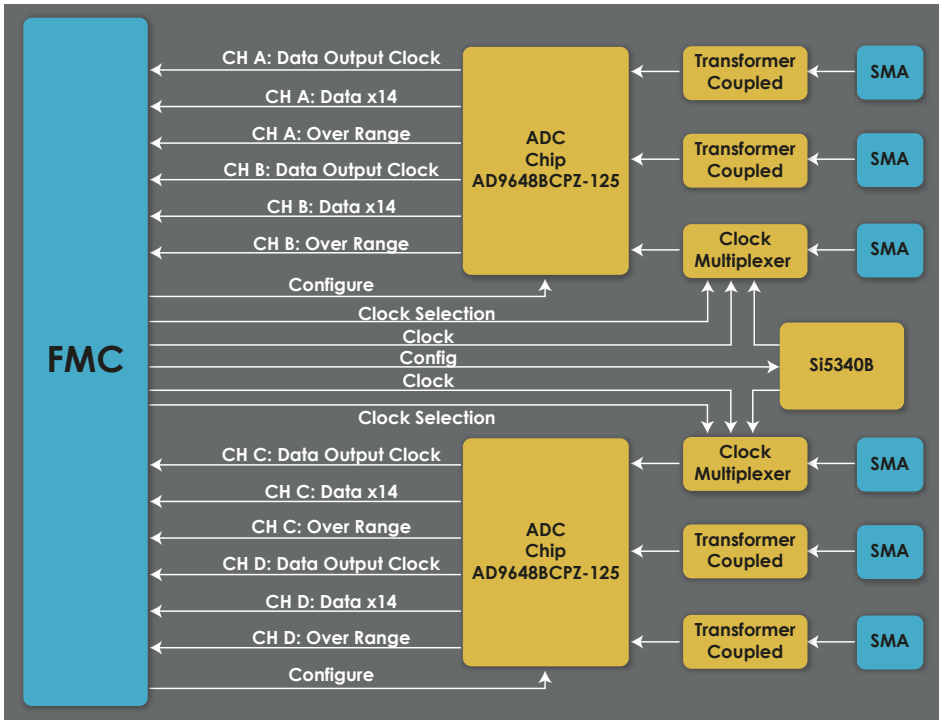
Hardware and Software Solution

- Terasic has a strong design expertise in FPGA hardware and software.
- Terasic creates FPGA-based products to meet our clients' specific requirements. We excel at delivering ready-to-use and highly-optimized systems. Terasic rugged FPGA systems have been deployed in various extreme environments, such as Wall Street's zero-downtime data centers and 5G base stations in desert.

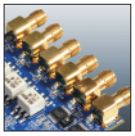
Consultancy Services

- At Terasic, we offer assistances to our clients in aspects such as porting, optimization, and benchmarking of applications executed on Terasic FPGA boards. Our support includes software upgrade and OpenCL design services.

Block Diagram



Specifications



- Two AD9648BCPZ-125 chips provide four high speed ADC ports (Con nected to 4 SMA connectors)
- Each channel can provide maximal 125 MSPS with 14-bits resolution data
- Clock Generator Si5340B. Default output 125MHz clock.
- Two SMA connectors for clock input
- Full Pin Count FMC interface
- Differential analog input with 650 MHz bandwidth
- 2 V p-p differential analog input
- Effective number of bits : between 11.4 ~ 11.9 Bits
- 1.8 V analog supply operation
- 1.8 V CMOS outputs
- SNR = 74.5 dBFS @ 70 MHz
- SFDR = 91 dBc @ 70 MHz
- Low power: 106 mW/channel @ 125 MSPS
- IF sampling frequencies to 200 MHz