ADC-FMC

User Manual

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Chapter 1

Introduction

The Terasic ADC-FMC is a four-channel high speed ADC daughter card with FMC interfaced. Two AD9648BCPZ-125 chips are used in this board. One AD9648BCPZ-125 chip can provide two ADC channels, and each channel can provide maximal 125 MSPS with 14-bits resolution data. The build-in onboard clock generator (Si5340B) provides the reference clock for the ADC chip. The reference clock of the ADC chip also can come from a FPGA via the on-board FMC connector or from an external clock source via the on-board SMA connector.

Note, the FPGA main board FMC interface will support VADJ 1.8V to work with ADC-FMC.

1.1 The Package Contents

The ADC-FMC kit comes with the following items:

- ADC-FMC Daughter Card
- Screw & Copper Pillar Package
- CD Download Guide

The system CD contains technical documents of the ADC-FMC kit, which include component datasheets, demonstrations, schematic and user manual. Users can download the CD from the link below:

http://adc-fmc.terasic.com/cd

Figure 1-1 shows the contents of the ADC-FMC kit.

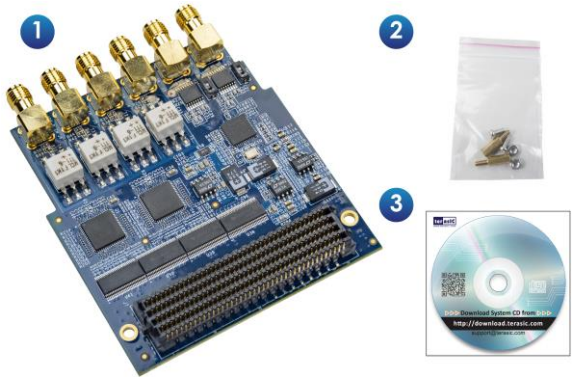

Figure 1-1 Contents of the ADC-FMC Kit

1.2 Assemble ADC-FMC with FPGA Mainboard

In order to make the ADC-FMC daughter card and the FMC connector on the FPGA mainboard with more secure hookup, the FMC side of the ADC-FMC daughter card has reserved two screw holes, as shown in **Figure 1-2**. Users can use the screws, copper pillars, and nuts that come with the ADC- FMC, to make the ADC-FMC secure on the FPGA mainboard, as shown in **Figure 1-3**. In order to use the ADC high-speed transmission in normal operation, we strongly recommend that users use the screws to secure the connection between the mainboard and the ADC-FMC card.

Figure 1-2 Two screw holds of the ADC-FMC

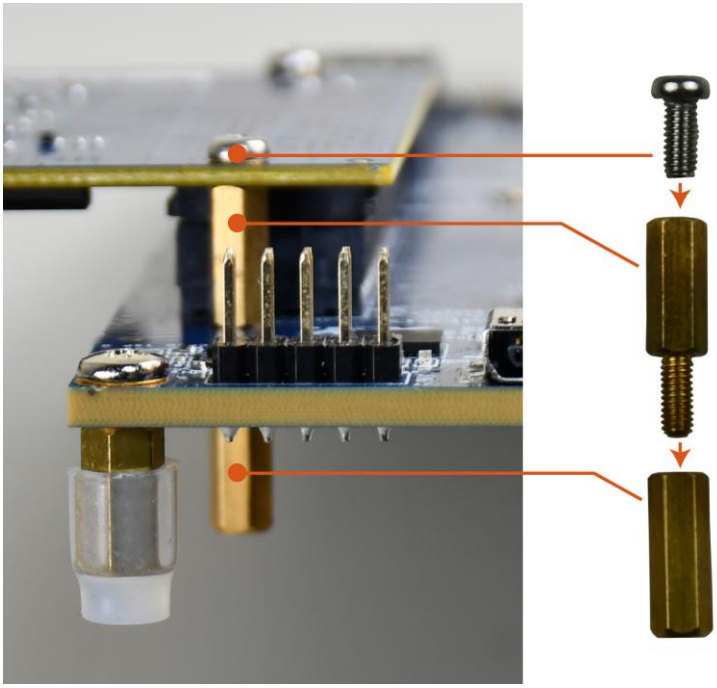

Figure 1-3 Installation of the ADC-FMC brackets

1.3 Connectivity

Figure 1-4 and Figure 1-5 below show the connectivity of the ADC-FMC to the TR5 and A5SoC FPGA boards. The ADC-FMC is powered from FPGA mainboard. It is not necessary to connect a power adapter to the ADC-FMC. There are four ADC channels on the ADC-FMC board. Full pin count FMC connector is required to utilized 4 ADC channel. If FPGA mainboard's FMC connector only supports low pin count, only two ADC channels can be used.

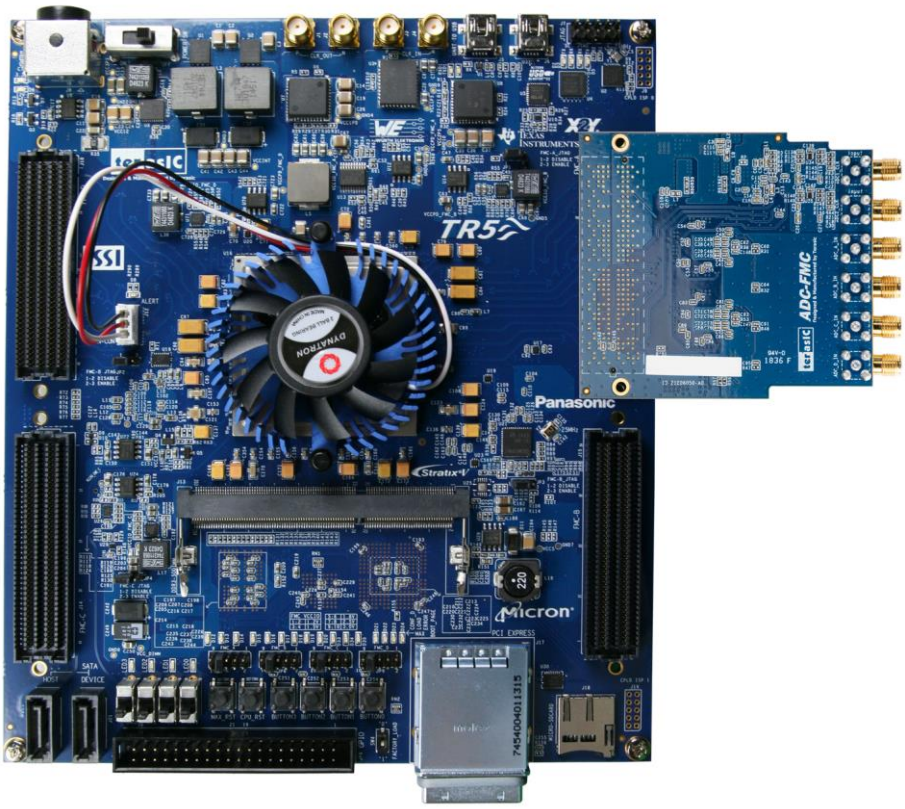

Figure 1-4 ADC-FMC with TR5

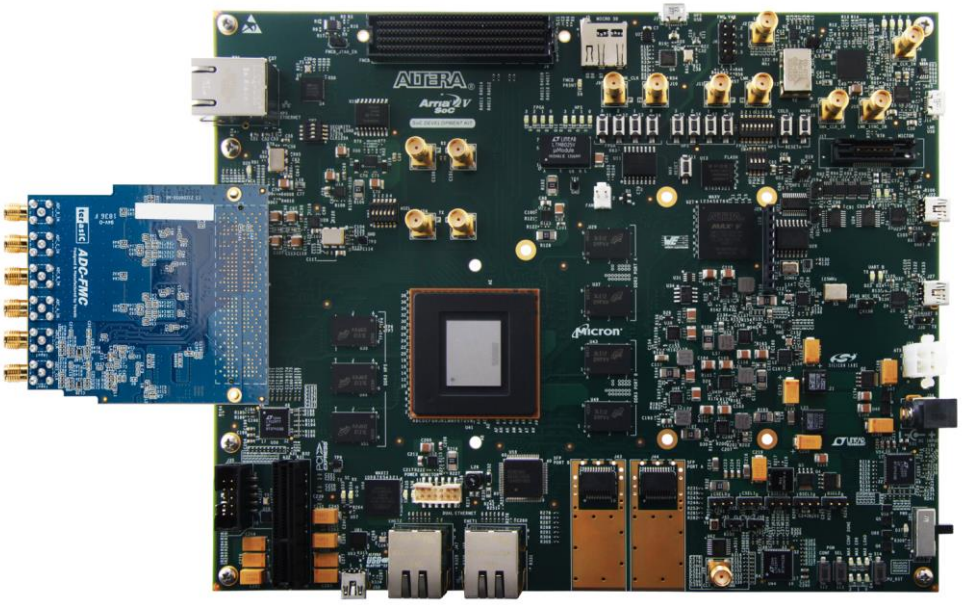

Figure 1-5 ADC-FMC with A5SoC

1.4 Getting Help

For Technical Support, Terasic's Contact Information is listed below:

- Office Hours: 9:00 a.m. to 6:00 p.m. (GMT +8)
- Telephone: +886-3-575-0880
- Email: support@terasic.com

Chapter 2

Architecture of ADC-FMC

This chapter lists the features and describes the architecture of ADC-FMC daughter card. There are four ADC channels on the board. Two channels utilize the low pin count of the FMC connector, and the other two channels utilized the high pin count of the FMC connector. To use four ADC channels, the mainboard's FMC connect must support 1.8V full pin count.

2.1 Features

The key features of this module are listed below:

- Four high speed ADC ports (Connected to 4 SMA connectors)
- ADC reference clock can come from on-board clock generator, FPGA main board or SMA connectors.
- Clock Generator Si5340B. Default output 125MHz clock.
- Two SMA connectors for clock input.
- FPC (Full Pin Count) FMC interface

2.2 Component and Layout

The top view of the ADC-FMC is shown in **Figure 2-1**.

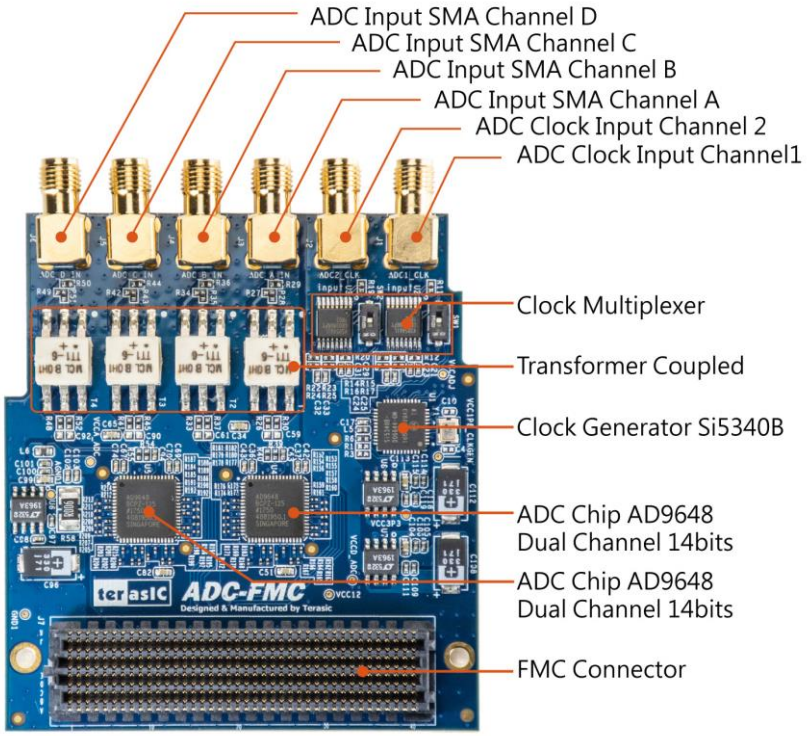

Figure 2-1 Top view of the ADC-FMC Daughter Card

The bottom view of the ADC-FMC is shown in **Figure 2-2**. It depicts the layout and indicates the locations of connectors and key components.

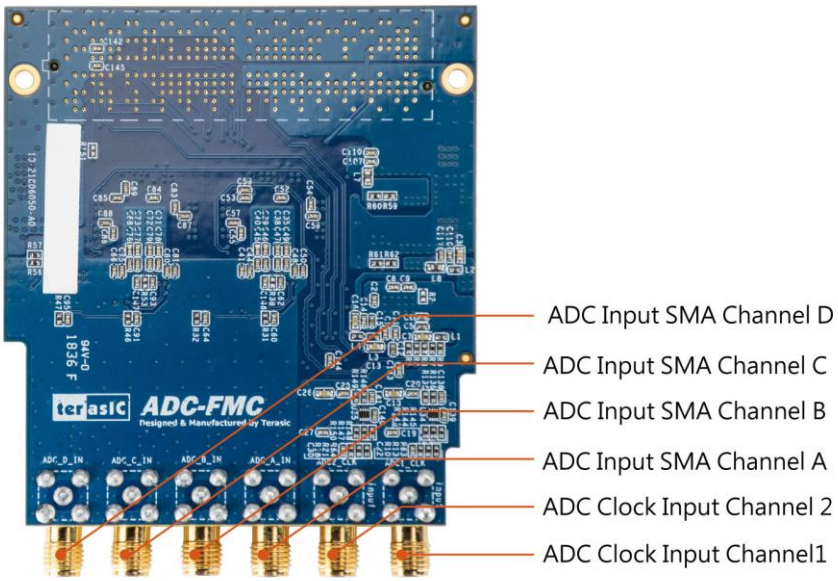

Figure 2-2 Bottom view of the ADC-FMC Daughter Card

2.3 Block Diagram

Figure 2-3 shows the block diagrams of the ADC-FMC. Two AD9648BCPZ-125 chips are used in this board. One AD9648BCPZ-125 chip can provide two ADC channels, and each channel can provide maximal 125 MSPS with 14-bits resolution data. The four analog inputs come from the on-board SMA connector.

The reference clock of the ADC chip can come from:

- on-board clock generator Si5340B,
- FPGA main board via FMC connector
- External clock source via SMA connectors.

The selection of clock sources is determined by a clock multiplexer chip 854S054AGILF. The on-board clock generator Si5340B default output 125MHz clock and developers can modify the output frequency via its I2C interface.

Note, the ADC Chips work on 1.8V voltage, so the developers must set the FMC VADJ as 1.8V in FPGA mainboard to avoid the board damaged.

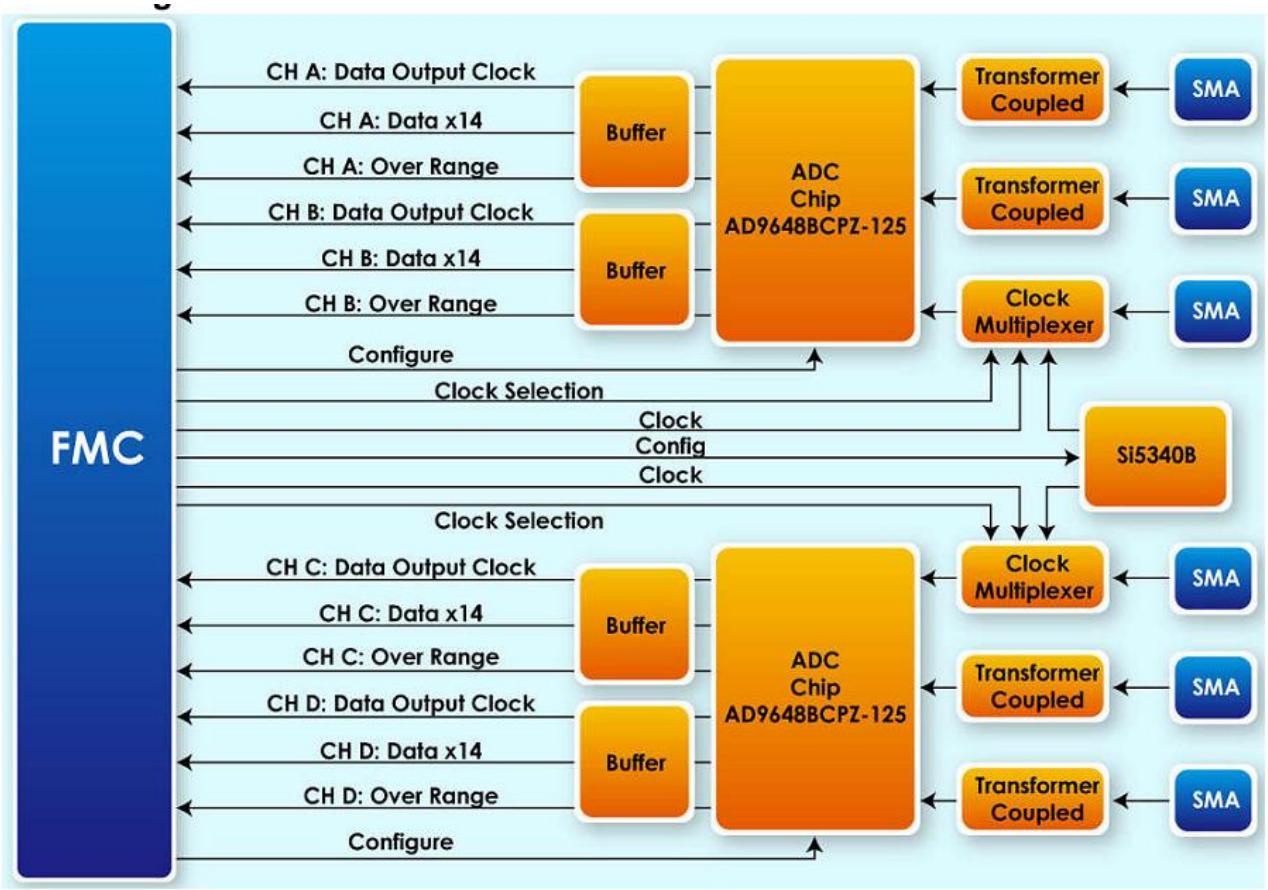

Figure 2-3 ADC-FMC Function in the Block Diagram

Chapter 3

Using the ADC-FMC

This chapter provides information on how to control the hardware of the ADC-FMC. It includes the definition of the FMC interface and how to use the ADC chips and clock generator hardware in the board.

Note, when using this board, remember FMC VCCADJ of main board must be set to 1.8V.

3.1 Pin Definition of FMC Connector

The FMC connector on the ADC-FMC daughter card connects directly to the FMC connector on the FPGA board. **Figure 3-1**, **Figure 3-2** and **Figure 3-3** illustrates the signal names of the FMC connector.

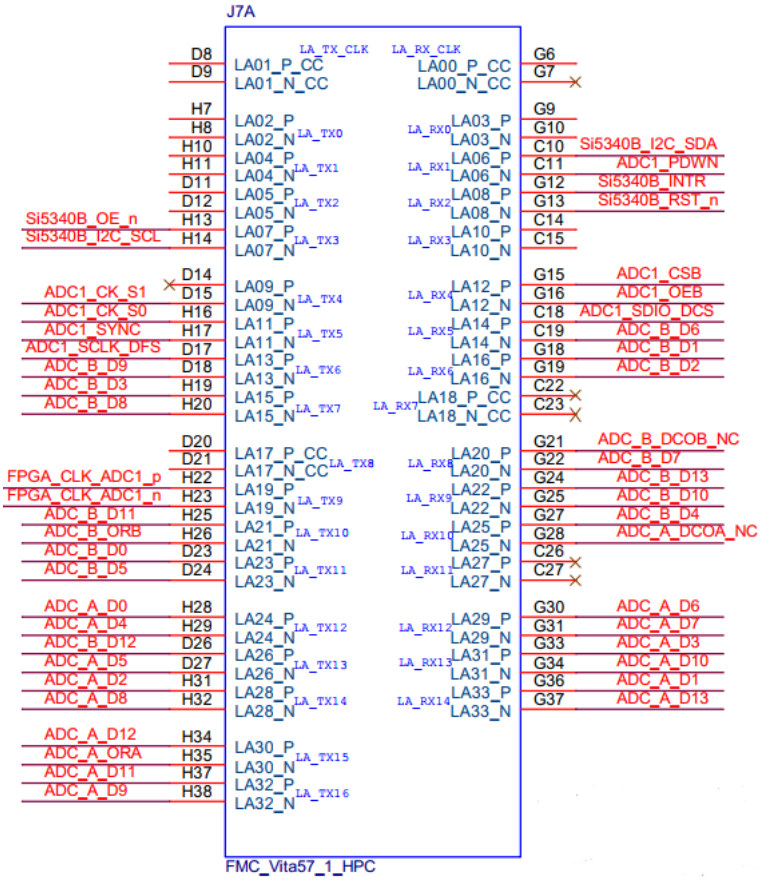

Figure 3-1 Signal names of FMC connector part 1

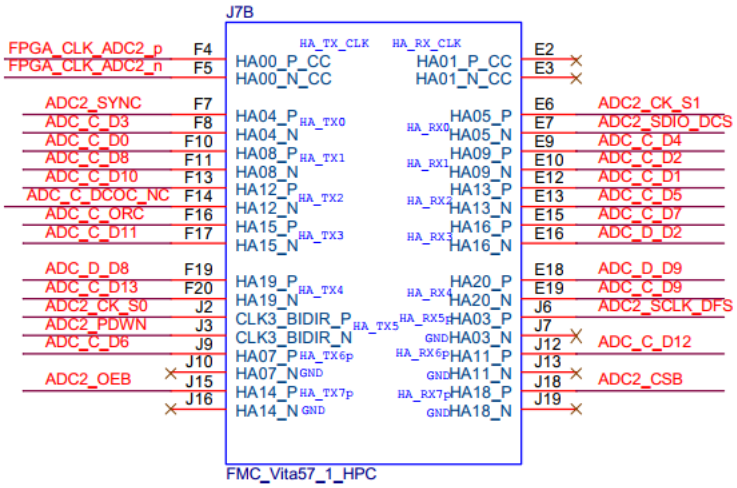

Figure 3-2 Signal names of FMC connector part 2

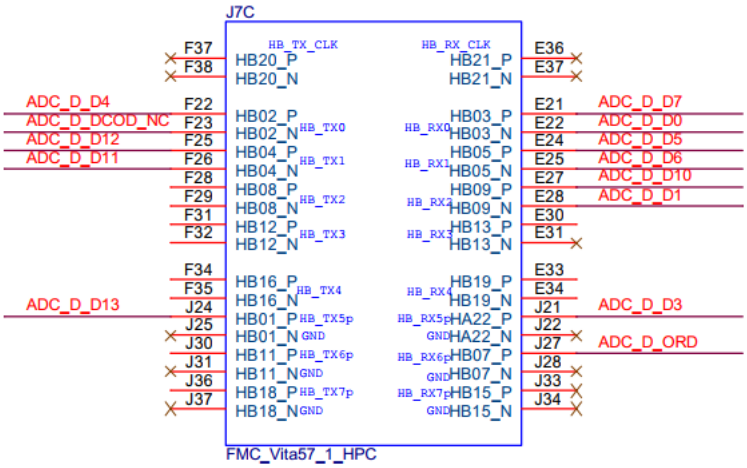

Figure 3-3 Signal names of FMC connector part 3

Table 3-1 shows the ADC-FMC pin assignments for the ADC-FMC pins in Quartus Prime.

Table 3-1 ADC-FMC Pin Assignments of FMC in Quartus Prime

Signal Name	*FMC Pin No.*	*Description*	*Direction*	*IO Standard*
ADC_A_D0	H28	First ADC Port-A Data0	input	VCCADJ
ADC_A_D1	G36	First ADC Port-A Data1	input	VCCADJ
ADC_A_D2	H31	First ADC Port-A Data2	input	VCCADJ
ADC_A_D3	G33	First ADC Port-A Data3	input	VCCADJ
ADC_A_D4	H29	First ADC Port-A Data4	input	VCCADJ
ADC_A_D5	D27	First ADC Port-A Data5	input	VCCADJ
ADC_A_D6	G30	First ADC Port-A Data6	input	VCCADJ
ADC_A_D7	G31	First ADC Port-A Data7	input	VCCADJ

ADC_A_D8	H32	First ADC Port-A Data8	input	VCCADJ
ADC_A_D9	H38	First ADC Port-A Data9	input	VCCADJ
ADC_A_D10	G34	First ADC Port-A Data10	input	VCCADJ
ADC_A_D11	H37	First ADC Port-A Data11	input	VCCADJ
ADC_A_D12	H34	First ADC Port-A Data12	input	VCCADJ
ADC_A_D13	G37	First ADC Port-A Data13	input	VCCADJ
ADC_A_DCOA	G28	First ADC Port-A Data Clock	input	VCCADJ
ADC_A_ORA	H35	First ADC Port-A Data Over range	input	VCCADJ
ADC_B_D0	D23	First ADC Port-B Data0	input	VCCADJ
ADC_B_D1	G18	First ADC Port-B Data1	input	VCCADJ
ADC_B_D2	G19	First ADC Port-B Data2	input	VCCADJ
ADC_B_D3	H19	First ADC Port-B Data3	input	VCCADJ
ADC_B_D4	G27	First ADC Port-B Data4	input	VCCADJ
ADC_B_D5	D24	First ADC Port-B Data5	input	VCCADJ
ADC_B_D6	C19	First ADC Port-B Data6	input	VCCADJ
ADC_B_D7	G22	First ADC Port-B Data7	input	VCCADJ
ADC_B_D8	H20	First ADC Port-B Data8	input	VCCADJ
ADC_B_D9	D18	First ADC Port-B Data9	input	VCCADJ
ADC_B_D10	G25	First ADC Port-B Data10	input	VCCADJ
ADC_B_D11	H25	First ADC Port-B Data11	input	VCCADJ
ADC_B_D12	D26	First ADC Port-B Data12	input	VCCADJ
ADC_B_D13	G24	First ADC Port-B Data13	input	VCCADJ
ADC_B_DCOB	G21	First ADC Port-B Data Clock	input	VCCADJ
ADC_B_ORB	H26	First ADC Port-B Data Over range	input	VCCADJ
ADC1_PDWN	C11		output	VCCADJ
ADC1_SDIO_DCS	C18	First ADC SPI Serial Data	inout	VCCADJ
ADC1_SCLK_DFS	D17	First ADC SPI Serial Clock	output	VCCADJ
ADC1_CSB	G15	First ADC SPI Chip Select (Active Low)	output	VCCADJ
ADC1_OEB	G16	First ADC Output Enable (Active Low)	output	VCCADJ
ADC1_SYNC	H17	First ADC Digital Synchronization	output	VCCADJ
ADC1_CK_S0	H16	First ADC Clock Selection bit0	output	VCCADJ
ADC1_CK_S1	D15	First ADC Clock Selection bit1	output	VCCADJ
FPGA_CLK_ADC1_p	H22	First ADC Clock source from FGPA	output	VCCADJ
ADC_C_D0	F10	Second ADC Port-A Data0	input	VCCADJ
ADC_C_D1	E12	Second ADC Port-A Data1	input	VCCADJ
ADC_C_D2	E10	Second ADC Port-A Data2	input	VCCADJ
ADC_C_D3	F8	Second ADC Port-A Data3	input	VCCADJ

ADC_C_D4	E9	Second ADC Port-A Data4	input	VCCADJ
ADC_C_D5	E13	Second ADC Port-A Data5	input	VCCADJ
ADC_C_D6	J9	Second ADC Port-A Data6	input	VCCADJ
ADC_C_D7	E15	Second ADC Port-A Data7	input	VCCADJ
ADC_C_D8	F11	Second ADC Port-A Data8	input	VCCADJ
ADC_C_D9	E19	Second ADC Port-A Data9	input	VCCADJ
ADC_C_D10	F13	Second ADC Port-A Data10	input	VCCADJ
ADC_C_D11	F17	Second ADC Port-A Data11	input	VCCADJ
ADC_C_D12	J12	Second ADC Port-A Data12	input	VCCADJ
ADC_C_D13	F20	Second ADC Port-A Data13	input	VCCADJ
ADC_C_DCOC	F14	Second ADC Port-A Data Clock	input	VCCADJ
ADC_C_ORC	F16	Second ADC Port-A Data Over range	input	VCCADJ
ADC_D_D0	E22	Second ADC Port-B Data0	input	VCCADJ
ADC_D_D1	E28	Second ADC Port-B Data1	input	VCCADJ
ADC_D_D2	E16	Second ADC Port-B Data2	input	VCCADJ
ADC_D_D3	J21	Second ADC Port-B Data3	input	VCCADJ
ADC_D_D4	F22	Second ADC Port-B Data4	input	VCCADJ
ADC_D_D5	E24	Second ADC Port-B Data5	input	VCCADJ
ADC_D_D6	E25	Second ADC Port-B Data6	input	VCCADJ
ADC_D_D7	E21	Second ADC Port-B Data7	input	VCCADJ
ADC_D_D8	F19	Second ADC Port-B Data8	input	VCCADJ
ADC_D_D9	E18	Second ADC Port-B Data9	input	VCCADJ
ADC_D_D10	E27	Second ADC Port-B Data10	input	VCCADJ
ADC_D_D11	F26	Second ADC Port-B Data11	input	VCCADJ
ADC_D_D12	F25	Second ADC Port-B Data12	input	VCCADJ
ADC_D_D13	J24	Second ADC Port-B Data13	input	VCCADJ
ADC_D_DCOD	F23	Second ADC Port-B Data Clock	input	VCCADJ
ADC_D_ORD	J27	Second ADC Port-B Data Over range	input	VCCADJ
ADC2_PDWN	J3		output	VCCADJ
ADC2_SDIO_DCS	E7	Second ADC SPI Serial Data	inout	VCCADJ
ADC2_SCLK_DFS	J6	Second ADC SPI Serial Clock	output	VCCADJ
ADC2_CSB	J18	Second ADC SPI Chip Select (Active Low)	output	VCCADJ
ADC2_OEB	J15	Second ADC Output Enable (Active Low)	output	VCCADJ
ADC2_SYNC	F7	Second ADC Digital Synchronization	output	VCCADJ
ADC2_CK_S0	J2	Second ADC Clock Selection bit0	output	VCCADJ
ADC2_CK_S1	E6	Second ADC Clock Selection	output	VCCADJ

		bit1		
FPGA_CLK_ADC2_p	F4	Second ADC Clock source from FGPA	output	VCCADJ
Si5340B_I2C_SCL	H14	Si5240B I2C Clock	inout	VCCADJ
Si5340B_I2C_SDA	C10	Si5240B I2C Data	inout	VCCADJ
Si5340B_INTR	G12	Si5240B Interrupt	input	VCCADJ
Si5340B_RST_n	G13	Si5240B Reset (Active Low)	output	VCCADJ
Si5340B_OE_n	H13	Si%340B Output Enable (Active Low)	output	VCCADJ

3.2 Using the ADC Chip AD9648BCPZ-125

Differential transformer-coupling is adapted as input configuration for the ADC chip, as shown in **Figure** 3-4. The input voltage should be 0~2.0 Voltage.

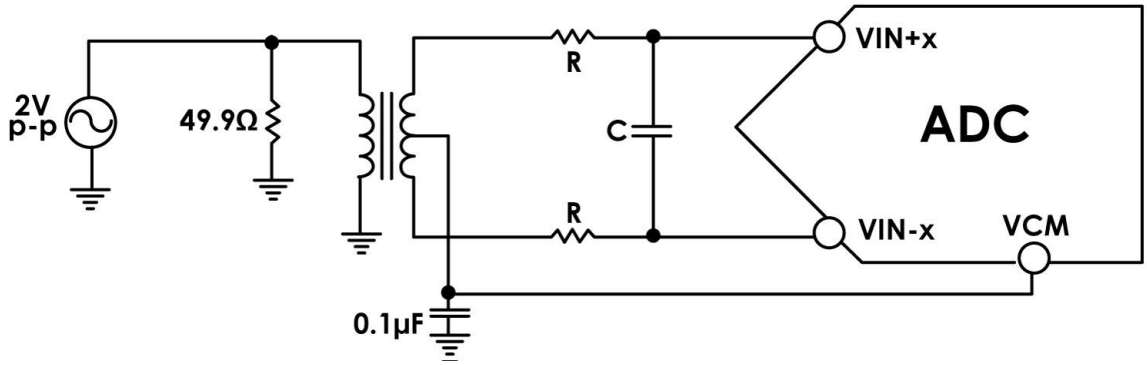

Figure 3-4 Differential Transformer-Coupled Configuration

Figure 3-5 shows the function block diagram of the ADC chip. Developers need to provide a reference clock to the differential clock input pins CLK+/CLK. The frequency of the reference clock determines the ADC sampling rate. There are two ADC blocks in the ADC chip. The digitalized data for the input analog VIN+A/VIN-A is output via the D0A~D14A 14 pins. Developers must lock the data based on the output clock DCOA. The ORA pin is used to indicate over-range output.

The ADC chip can be configured via its SPI interface. The default ADC sampling rate is equal to the frequency of the reference clock CLK+/CLK-. Developers can modify the DIVIDE register to change the ratio between reference clock frequency and sampling rate.

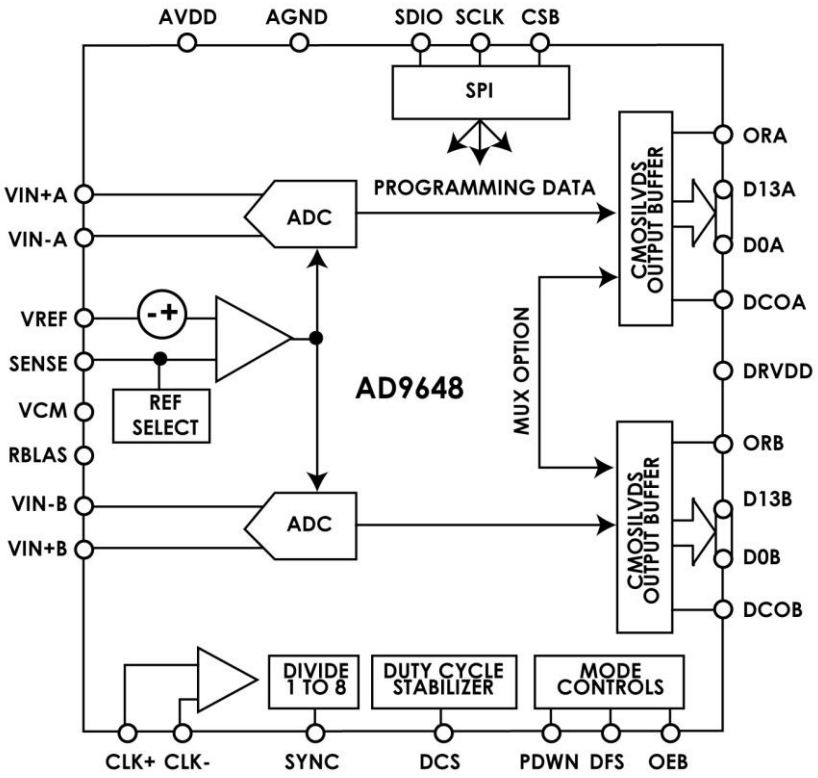

Figure 3-5 Block Diagram of AD9648

3.3 Select reference clock source for ADC

There are three clock sources available for the ADC chip:

- on-board clock generator Si5340B,
- FPGA main board via FMC connector
- External clock source via SMA connectors.

Developers can dynamic select the clock source via the ADC1_CK_S0/S1 pins for the first ADC chip and the ADC2_CK_S0/S1 pins for the second ADC chip, as shown in **Table 3-2**.

Table 3-2 Clock Source Selection

S1/S0	Clock Source
0/0	Si5340B
0/1	SMA
1/0	FPGA

In default, Si5340B outputs 125MHz clock on OUT0 and OUT1 port. OUT0 provides reference clock for the first ADC chip, and OUT1 provides reference clock for the second ADC chip. Developers can modify the output frequency by configure Si5340B via its I2C interface.

If SMA clock source is selected, developers need to provide clock source via SMA connector. On-board SW1 and SW2 are designed to specify the voltage range of clock input to SMA connector. When switches are off, the input clock voltage is expected to 3.3V. When switches are on, the input clock voltage is expected to 2.5V.

If FPGA clock source is selected, developers need to provide difference clock source to FPGA_CLK_ADC1_p/n and FPGA_CLK_ADC2_p/n.

Chapter 4

ADC Demonstrations

This chapter shows how to configure ADC chips via SPI interface and retrieve the digitalized values from the ADC channels.

Note, remember FMC VCCADJ of the main board must be set to 1.8V to avoid board damaged.

4.1 Demo Block Diagram

Figure 4-1 shows the block diagram of this demonstration. Four FIFO are used to store the retrieved digitalized values from four ADC Channels. Data output of each ADC channel has an associated FIFO to store the data. Each FIFO is configured as separated input clock and output clock, 14bits width, and 32 words depth. The data and clock output of each ADC channel is connected to write clock and data input of the associated FIFO. One of the four data clock outputs are connected to the write clock inputs of the four FIFO and selected as sampling clock in Signal Tap Logic Analyzer. The output data of each FIFO is selected as sampling data in Signal Tap Logic Analyzer.

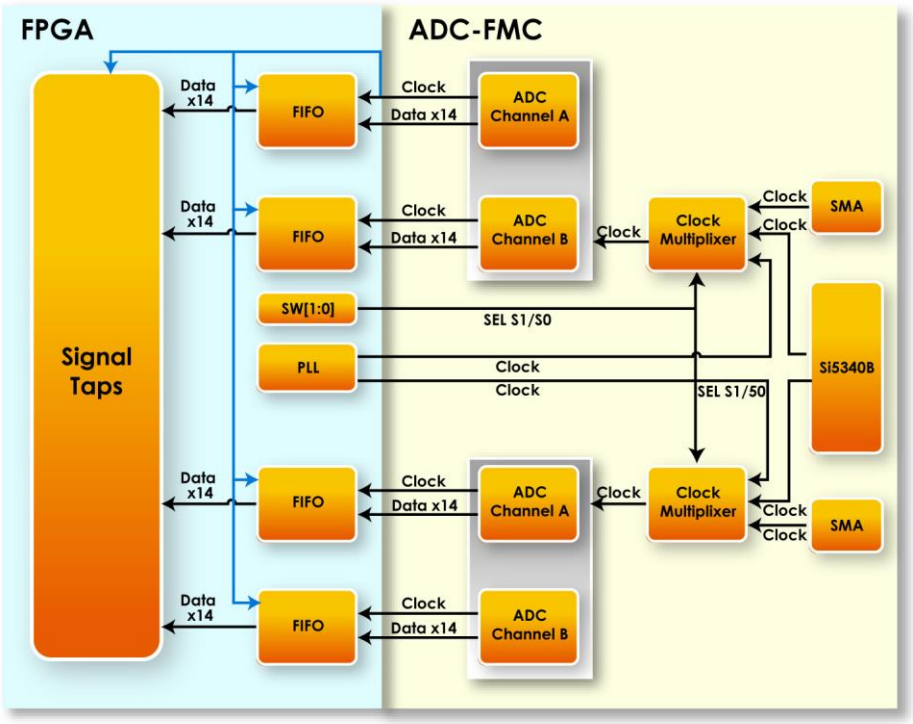

Figure 4-1 Block Diagram of Demonstration

SWITCH[1:0] on FPGA main board is used to select reference clock source for ADC Chips. Width SWITCH[1:0]=0, Si5340B default output 125Mhz is used as reference clock of the ADC Chips. With SWITCH[1:0]=1, external clock coming from SMA is used. In this case, users need to provide clock source to the SMA connector. Besides, users have to adjust the SW1 and SW2 on ADC-FMC board according to voltage range of the external clock source. With SWITCH[1:0]=2, ADC will get reference the clock which is coming from FPGA PLL.

4.2 Demo on TR5 FPGA Mainboard

This section shows how to setup the demo on the Terasic TR5 FPGA Board. TR5 FMC-A connector is used to connect the ADC-FMC board in this demo. User also can use FMC-D connector on TR5. FMC-B and FMC-C on TR5 are not recommended because they are low pin count FPGA connectors, only two ADC channels can be used.

■ Hardware Setup

Figure 4-2 shows the demo setup of ADC-FMC with TR5 mainboard. The ADC-FMC should be installed on the FMC-A expansion header of the TR5. Adjust the VADJ of MFC-A connector to be 1.8V.

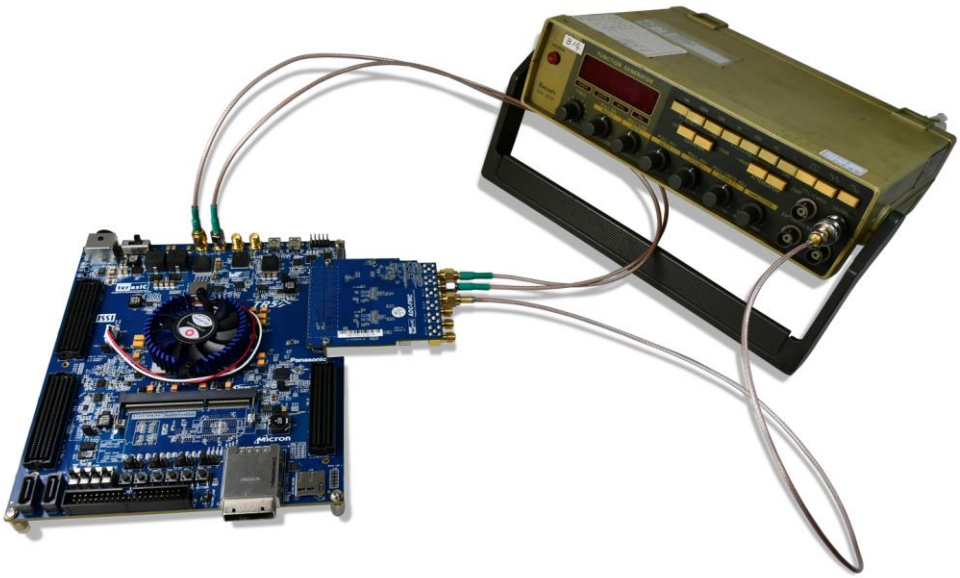

Figure 4-2 Hardware setup of ADC-FMC with TR5

■ Execute Demonstration

Please follow the procedures below to setup the demonstration:

1. Power off the TR5.
2. Make sure the ADC-FMC is installed as shown in Figure 4-2. The signals to be measured can generate from Analog signal generator. Users can connect the output port of the

generator to the ADC_A_IN/ADC_B_IN/ADC_C_IN/ADC_D_IN port of the ADC-FMC card through SMA cable (The output frequency should be more than 100KHz). The ADC1_CLK and ADC2_CLK are come from two options below:

a) TR5_CLK_OUT: Connect ADC1_CLK on ADC_FMC card to CLK_OUT_p (J1) on TR5 board, and connect ADC2_CLK on ADC-FMC card to CLK_OUT_n (J2) on TR5 board. Set the SW1/SW2 on ADC-FMC card as ON.
b) External 125MHz clock generator: Set the SW1/SW2 on ADC-FMC card as OFF if the clock generator output signal is 3.3V standard, or set SW1/SW2 as ON if the output signal is 2.5V.

3. Make sure the FMC_A VADJ is set to 1.8V by shorting J5.7 and J5.8 as shown in **Figure 4-3**.
4. Connect the USB Blaster II USB port J6 of the TR5 to the USB port of host PC with a Mini USB cable.
5. Power on the TR5 FPGA board.
6. Make sure Quartus Prime and USB-Blaster II driver has been installed on the host PC.
7. Copy the folder Demonstrations\TR5_ADC-FMCA\demo_batch from the ADC-FMC System CD to the host PC and execute "test.bat" to configure the FPGA.
8. Set SW[1:0] to 00 as shown in **Figure 4-4**.
9. Double click "freq.stp" to launch Signal Tap Logic Analyzer.
10. Click Start button on Signal Tap Windows, the ADC waveform will appear as shown in **Figure 4-5**. (It shows four channels Sine wave, because the four channels of the Analog signal generator are all connected to the four ADC_In ports. If only one channel signal is connected, only one sine wave will be shown in Signal Tap Logic Analyzer).
11. Optionally, change SW[1:0] setting to select deference reference clock source for ADC chips.

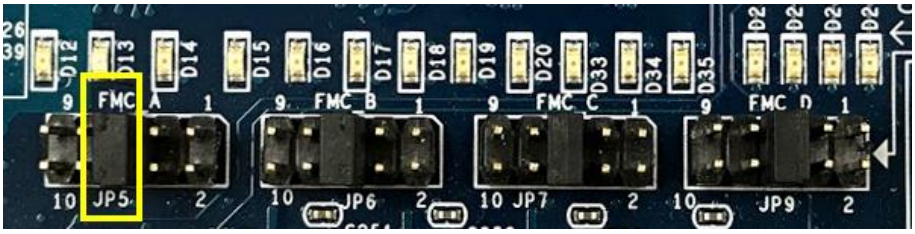

Figure 4-3 Short J5.7 and J5.8

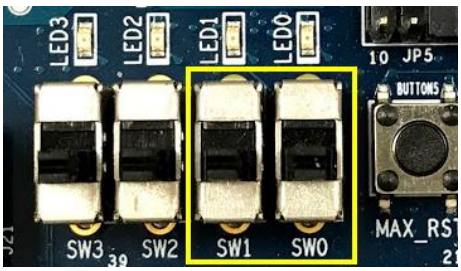

Figure 4-4 SWITCH[1:0] on TR5

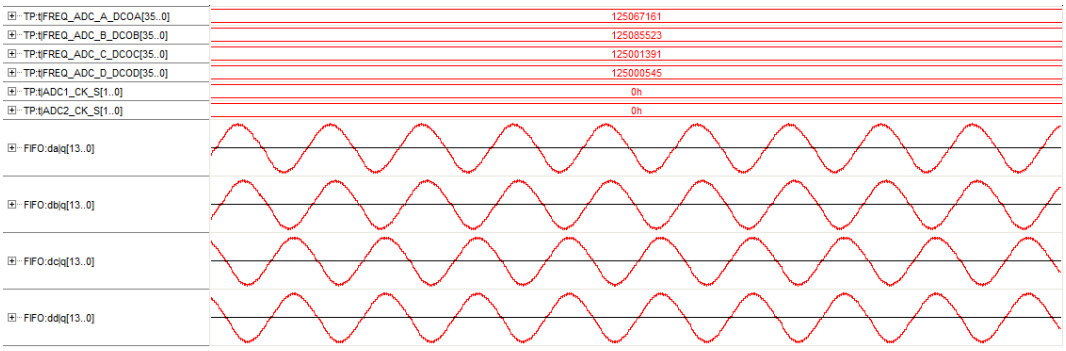

Figure 4-5 Signal Tap Logic Analyzer for TR5

■ Project Source Code

The source code of Quartus project for the ADC demo with the TR5 board is available in the "Demonstrations\ TR5_ADC-FMCA" folder from the ADC-FMC System CD.

4.3 Demo on Intel A5SoC FPGA Mainboard

This section shows how to setup the demo on the Intel A5SoC FPGA Board. A5SoC FMC-A connector is used to connect the ADC-FMC board in this demo. User also can use FMC-B connector on A5SoC. Both FMC connectors on A5SoC are low pin count, so only two ADC channels can be used.

■ Hardware Setup

Figure 4-6 shows the demo the setup of ADC-FMC with A5SoC mainboard. The ADC-FMC should be installed on the FMC-A expansion header of the A5SoC. Adjust the VADJ of MFC-A connector to be 1.8V.

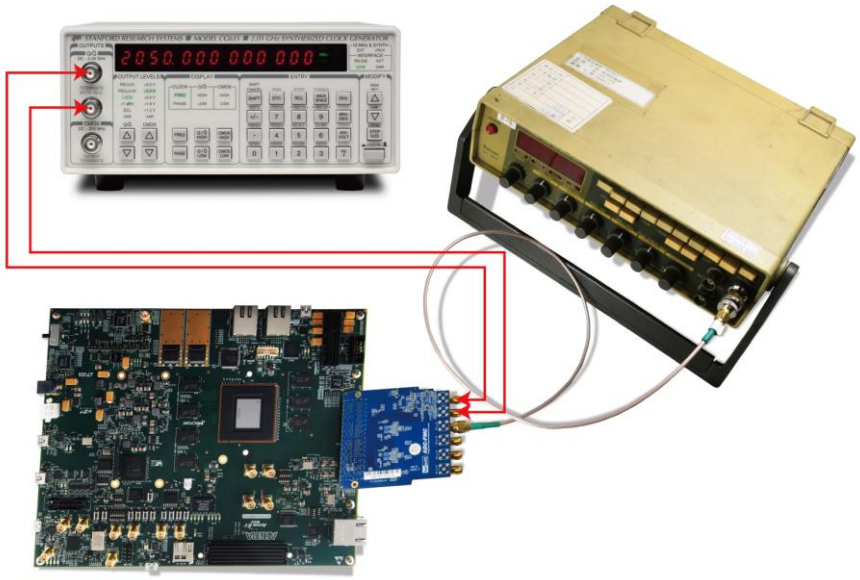

Figure 4-6 Hardware setup of ADC-FMC with A5SoC

■ Execute Demonstration

Please follow the procedures below to setup the demonstration:

1. Power off the A5SoC.
2. Make sure the ADC-FMC is installed as shown in **Figure 4-6**. Users can connect the output port of the generator to the ADC_A_IN/ADC_B_IN/ADC_C_IN/ADC_D_IN port of the ADC-FMC card through SMA cable (The output frequency should be more than 100KHz). Connect ADC1_CLK and ADC2_CLK on ADC-FMC card to external 125MHz clock generator through two SMA cables. Set the SW1/SW2 on ADC-FMC card as OFF if the clock generator output signal is 3.3V standard, or set SW1/SW2 as ON if the output signal is 2.5V.
3. Make sure the FMC VAR J6 is set to 1.8V as shown in **Figure 4-7**.
4. Connect the USB Blaster II USB port J50 of the A5SoC to the USB port of host PC with a Mini USB cable.
5. Power on the A5SoC FPGA board.
6. Make sure Quartus Prime and USB-Blaster II driver has been installed on the host PC.
7. Copy the folder Demonstrations\A5SoC_ADC-FMCA\demo_batch from the ADC-FMC System CD to the host PC and execute “test.bat” to configure the FPGA.
8. Set SW[1:0] to 00 as shown in **Figure 4-8**.
9. Double click “freq.stp” to launch Signal Tap Logic Analyzer.
10. Click Start button on Signal Tap Windows, the ADC waveform will appear.
11. Optionally, change SW[1:0] setting to select deference reference clock source for the ADC chips.

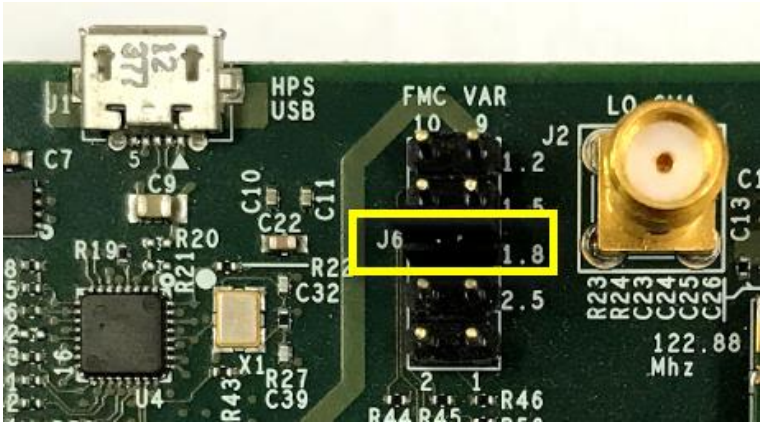

Figure 4-7 Select 1.8V on J6 FMC VAR

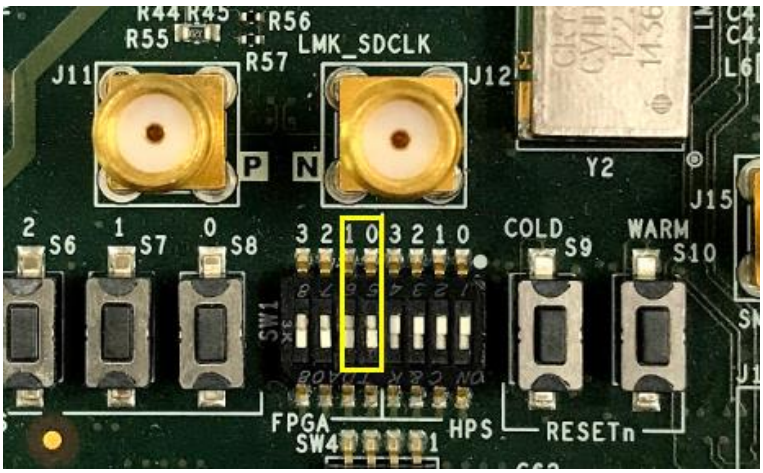

Figure 4-8 SWITCH[1:0] on A5SoC

■ Project Source Code

The source code of Quartus project for the ADC demo with the A5SoC board is available in the "Demonstrations\A5SoC_ADC-FMCA" folder from the ADC-FMC System CD.

4.4 Demo on Terasic HAN Board

This section shows how to setup the demo on the Terasoc HAN Board. The FMC connector of the HAN board is used to connect the ADC-FMC card in this demonstration.

■ Hardware Setup

Figure 4-9 shows the demo the setup of ADC-FMC with HAN board. The ADC-FMC should be installed on the FMC expansion header of the HAN. Adjust the VADJ of MFC connector to be 1.8V.

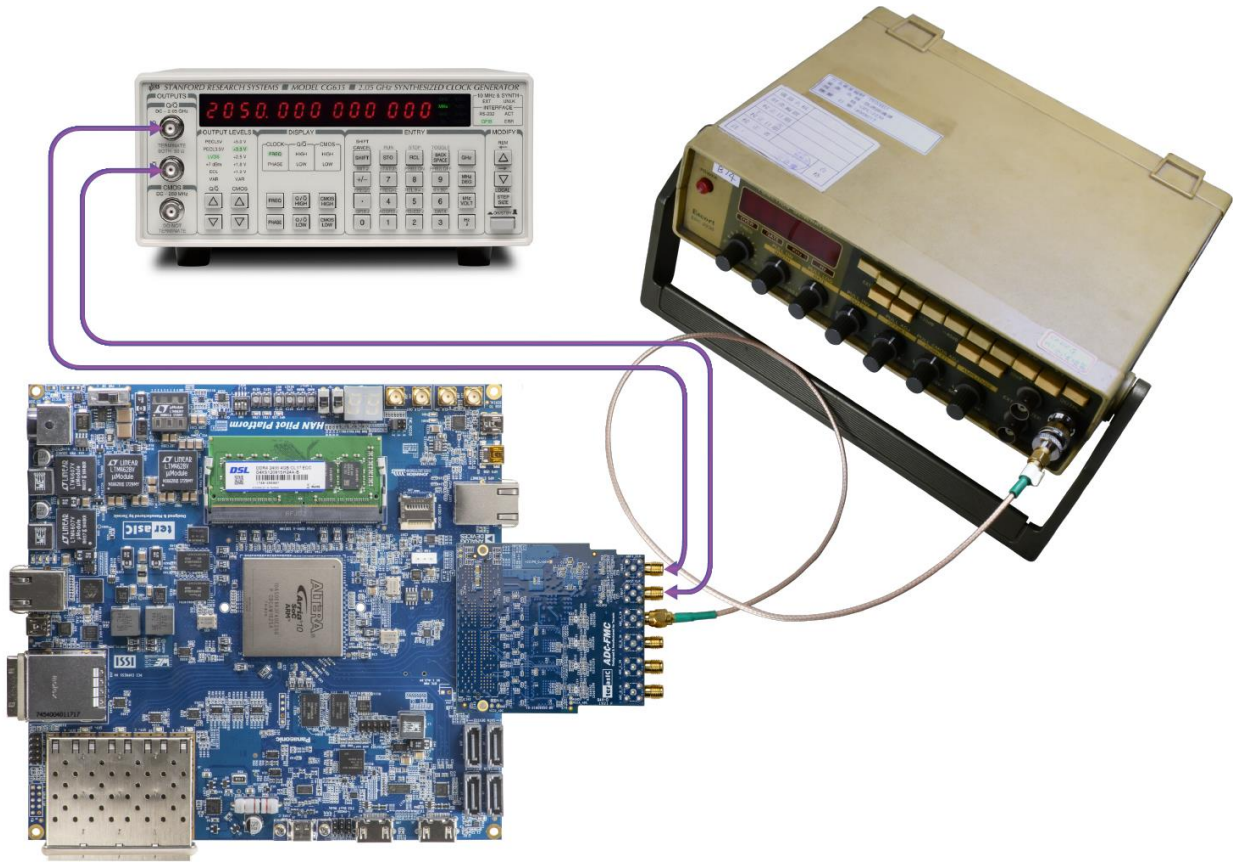

Figure 4-9 Hardware setup of ADC-FMC with HAN

■ Project Source Code

The source code of Quartus project for the ADC demo with the HAN board is available in the "Demonstrations\HAN_ADC-FMC" folder from the ADC-FMC System CD.

■ Execute Demonstration

Please follow the procedures below to setup the demonstration:

1. Power off the HAN.
2. Make sure the ADC-FMC is installed on the HAN as shown in **Figure 4-9.**
3. Users can connect the output port of the generator to the ADC_A_IN/ADC_B_IN/ADC_C_IN/ADC_D_IN port of the ADC-FMC card through SMA cable (The output frequency should be more than 100KHz). Connect ADC1_CLK and ADC2_CLK on ADC-FMC card to external 125MHz clock generator through two SMA cables. Set the SW1/SW2 on ADC-FMC card as OFF if the clock generator output signal is 3.3V voltage level, or set SW1/SW2 as ON if the output signal is 2.5V.
4. Make sure the FMC_VCCIO switch **JP2** of the HAN is set to 1.8V as shown in **Figure 4-10.**

5. Connect the Mini-USB port J20 of the HAN to the USB port of host PC with a Mini USB cable.
6. Power on the HAN board.
7. Make sure Quartus Prime and USB-Blaster II driver has been installed on the host PC.
8. Copy the folder Demonstrations\HAN_ADC-FMC\demo_batch from the ADC-FMC System CD to the host PC and execute “test.bat” to configure the FPGA.
9. Set SW[1:0] of the HAN board to ”00” as shown in **Figure 4-11**.
10. Double click “freq.stp” in the demo_batch folder to launch Signal Tap Logic Analyzer.
11. Click Start button on Signal Tap Windows, the ADC waveform will appear.
12. Optionally, change SW[1:0] setting to select deference reference clock source for the ADC chips.

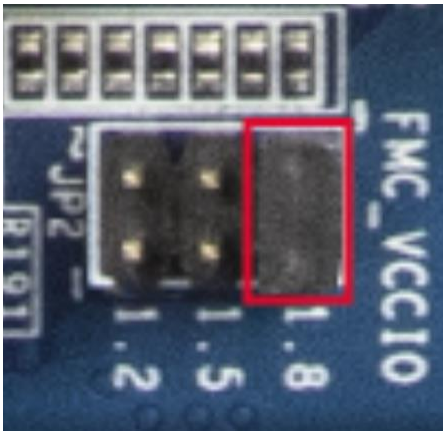

Figure 4-10 Select 1.8V on JP2 VCCIO_FMC VAR

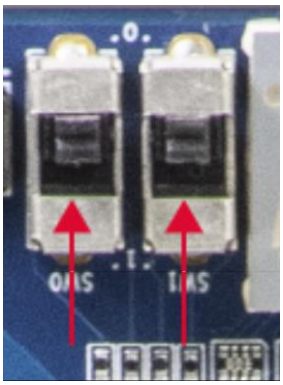

Figure 4-11 SW0[1:0] on HAN

4.5 Demo on Apollo S10 SoM Board

This section shows how to setup the demo on the Terasoc Apollo S10 SoM Board. The FMC connector of the Apollo S10 SoM board is used to connect the ADC-FMC card in this demonstration.

■ Hardware Setup

Figure 4-12 shows the demo the setup of ADC-FMC with Apollo S10 SoM. The ADC-FMC card should be installed on the FMC expansion header of the Apollo S10 SoM. Please adjust the VADJ of MFC connector to be 1.8V (See the user manual's section 2.2 of the Apollo S10 SoM).

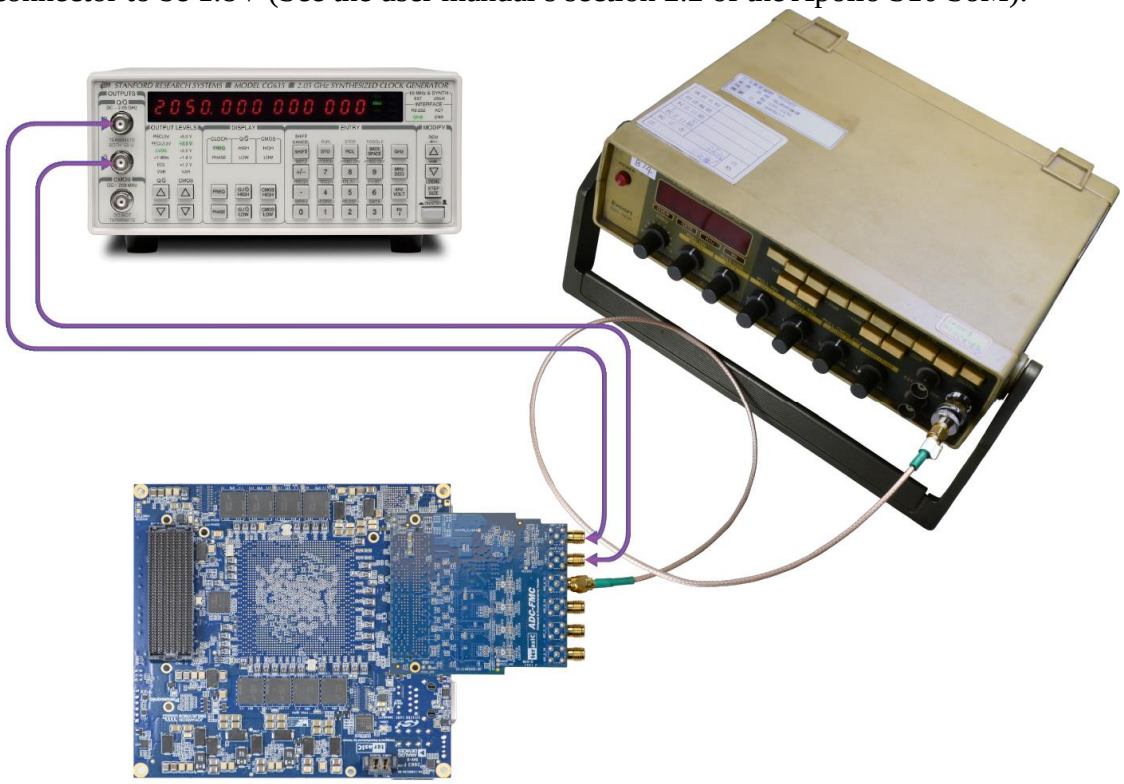

Figure 4-12 Hardware setup of ADC-FMC with Apollo S10 SoM

■ Project Source Code

The source code of Quartus project for the ADC demo with the Apollo S10 SoM board is available in the "Demonstrations\S10_ADC_FMC" folder from the ADC-FMC System CD.

■ Execute Demonstration

Please follow the procedures below to setup the demonstration:

13. Power off the Apollo S10 SoM.
14. Make sure the ADC-FMC is installed on the Apollo S10 SoM as shown in Figure 4-12.
15. Users can connect the output port of the generator to the ADC_A_IN/ADC_B_IN/ADC_C_IN/ADC_D_IN port of the ADC-FMC card through SMA cable (The output frequency should be more than 100KHz). Connect ADC1_CLK and ADC2_CLK on ADC-FMC card to external 125MHz clock generator through two SMA

cables. Set the SW1/SW2 on ADC-FMC card as OFF if the clock generator output signal is 3.3V voltage level, or set SW1/SW2 as ON if the output signal is 2.5V.

16. Make sure the VCCIO_FMC VAR **JP2** of the Apollo S10 SoM is set to 1.8V as shown in **Figure 4-13**.
17. Connect the Mini-USB port J8 of the Apollo S10 SoM to the USB port of host PC with a Mini USB cable.
18. Power on the Apollo S10 SoM board.
19. Make sure Quartus Prime and USB-Blaster II driver has been installed on the host PC.
20. Copy the folder Demonstrations\S10_ADC_FMC\demo_batch from the ADC-FMC System CD to the host PC and execute “test.bat” to configure the FPGA.
21. Set SW0[1:0] of the Apollo SoM to ”00” as shown in **Figure 4-14**.
22. Double click “freq.stp” in the demo_batch folder to launch Signal Tap Logic Analyzer.
23. Click Start button on Signal Tap Windows, the ADC waveform will appear.
24. Optionally, change SW0[1:0] setting to select deference reference clock source for the ADC chips.

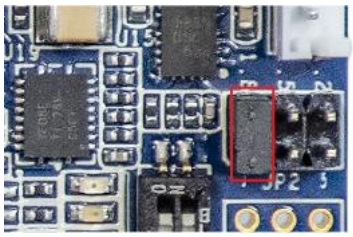

Figure 4-13 Select 1.8V on JP2 VCCIO_FMC VAR

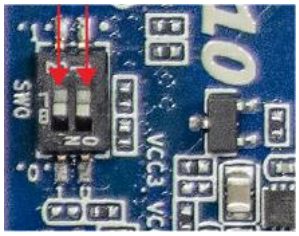

Figure 4-14 SW0[1:0] on Apollo S10 SoM

Chapter 5

Appendix

5.1 Revision History

Version	Date	Change Log
V1.0	10/24, 2018	Initial Version (Preliminary)
V1.1	07/18, 2019	Update for rev B (Adding buffer)
V1.2	04/24, 2020	Modify Figure 3-1,3-2,3-3 and Table 3-1
V1.3	11/24,2020	Add section 4.4 and 4.5
V1.4	05/302024	Modify block diagram

5.2 Copyright Statement