LCD Multimedia HSMC v2.0

Reference Manual

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Contents

Additional Information

1. Overview

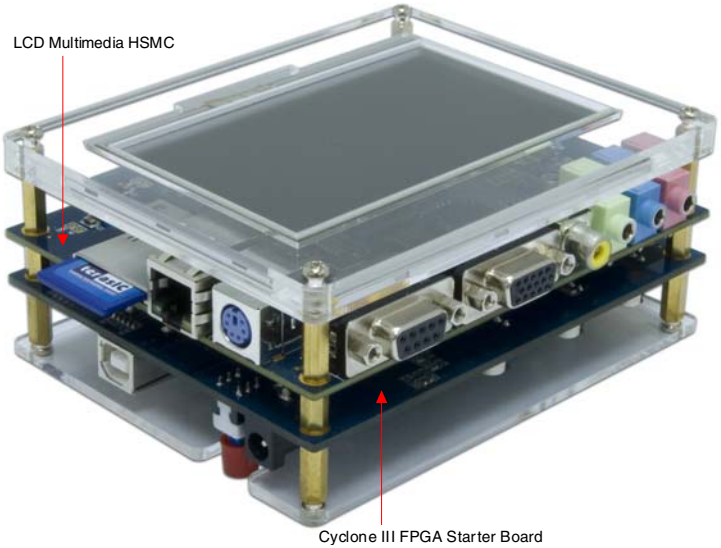
General Description

This manual provides comprehensive information about the LCD Multimedia High Speed Mezzanine Card version 2.0 (HSMC). This HSMC is a full-featured multimedia board that can be used for video, audio, and ethernet applications with many of the Altera FPGA Starter and Development boards that support the HSMC connectors. For example, see Figures 1–1.

The LCD Multimedia HSMC was created to provide a set of interfaces including LCD touchscreen, VGA out, composite video in, audio in/out, microphone in, plus Ethernet, SD-Card, PS/2, and RS-232 interfaces. The purpose of this reference manual is to describe each of these hardware interfaces on the LCD HSMC.

For the latest information about available HSMC boards, go to **www.altera.com/products/devkits/kit-index.html**.

Figure 1–1. LCD Multimedia HSMC in Nios II Embedded Evaluation Kit

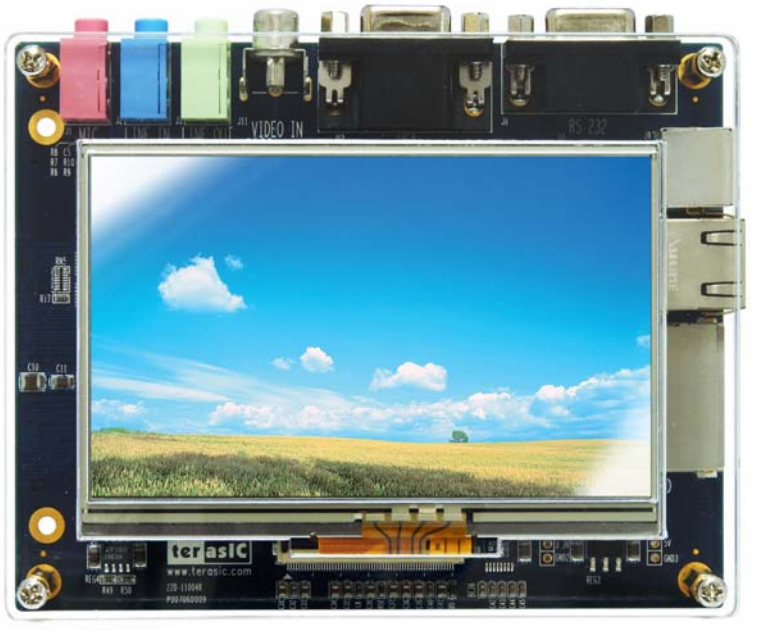


The top view of the LCD Multimedia HSMC is shown in Figure 1–2.

There are several sample software applications that highlight the LCD Touchpanel, SD-Card, and Ethernet components of the LCD Multimedia HSMC in the Nios II Development Kits.

For more information, refer *Nios II Embedded Evaluation kit Getting Started User Guide* as an example.

Figure 1–2. Top View of the LCD Multimedia HSMC



Connector view1 and connector view2 of the LCD Multimedia HSMC is shown in Figure 1–3 and Figure 1–4.

Figure 1–3. LCD Multimedia HSMC Side View 1

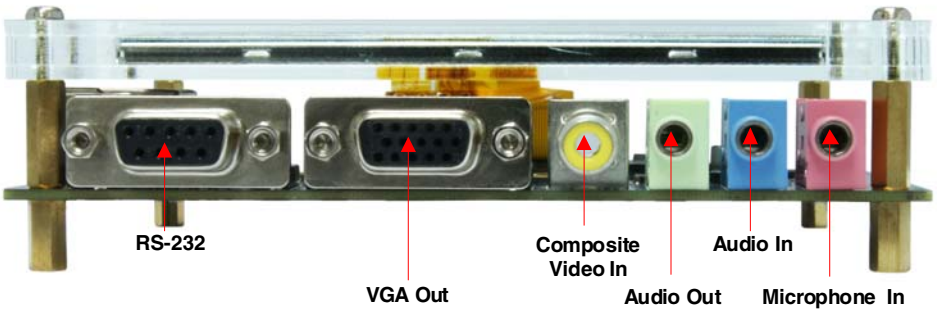
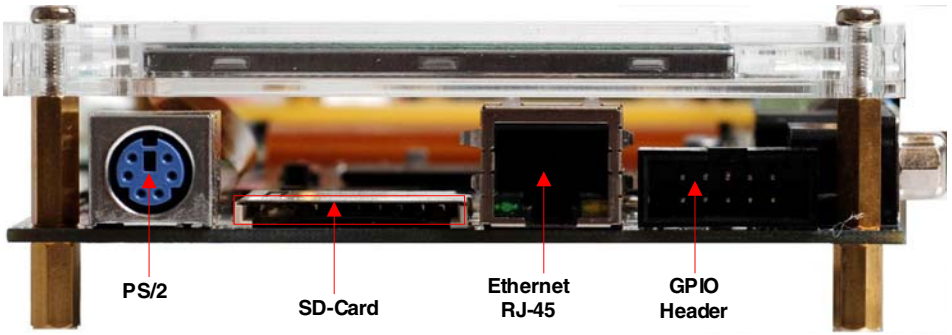


Figure 1–4. LCD Multimedia HSMC Side View 2



Components and Block Diagram

The LCD Multimedia HSMC contains the following components.

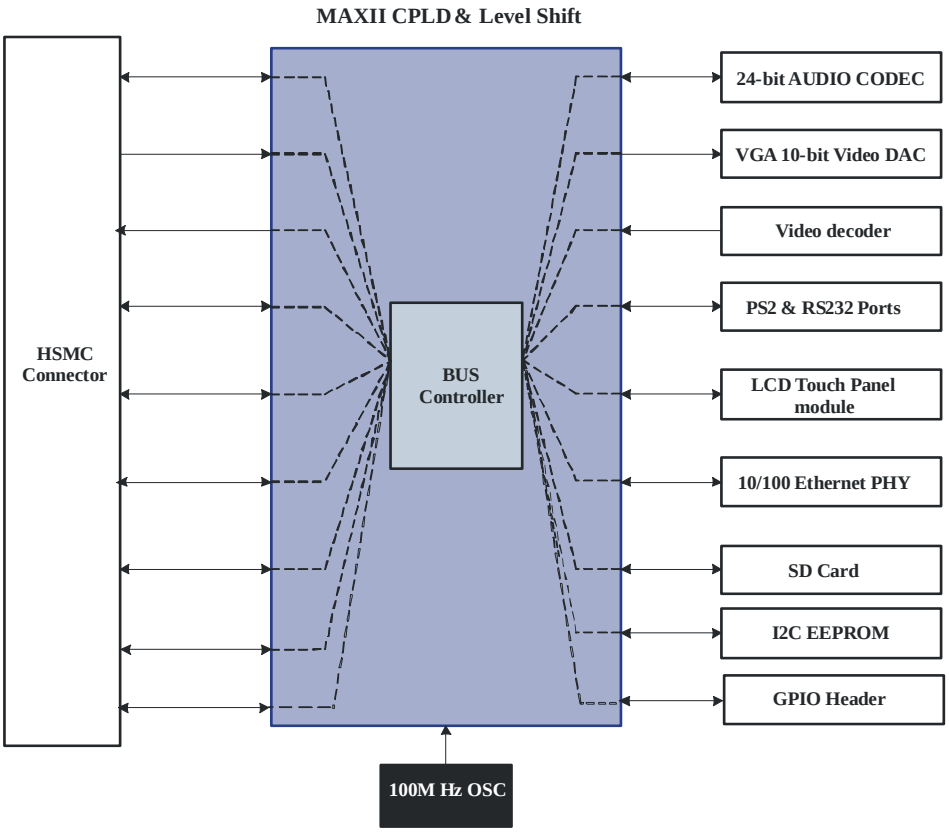
- MAX II CPLD EPM2210F324
  - 2210 Logic elements
  - 272 User I/Os
  - 324 pin FineLine BGA package
- LCD Touch-screen Display
  - 800 X 480 pixel 4.3" Display
- 24-bit Audio Codec
- SD Flash Connector
- 10/100 Ethernet physical layer (PHY)

- PS/2 Connector
- Other Interfaces
  - RS-232 Level-shifters
  - RCA Jack (Video In)
  - 10-bit VGA Output DAC
  - Composite Video ADC
  - General Purpose I/O (version 2.0)

Block Diagram

Figure 1–5 shows a functional block diagram of the LCD Multimedia HSMC.

Figure 1–5. LCD Multimedia HSMC



2. Board Components and Interfaces

Board Overview

This chapter provides operational and connectivity detail for the LCD Multimedia HSMC's major components and interfaces and is divided into the following major blocks:

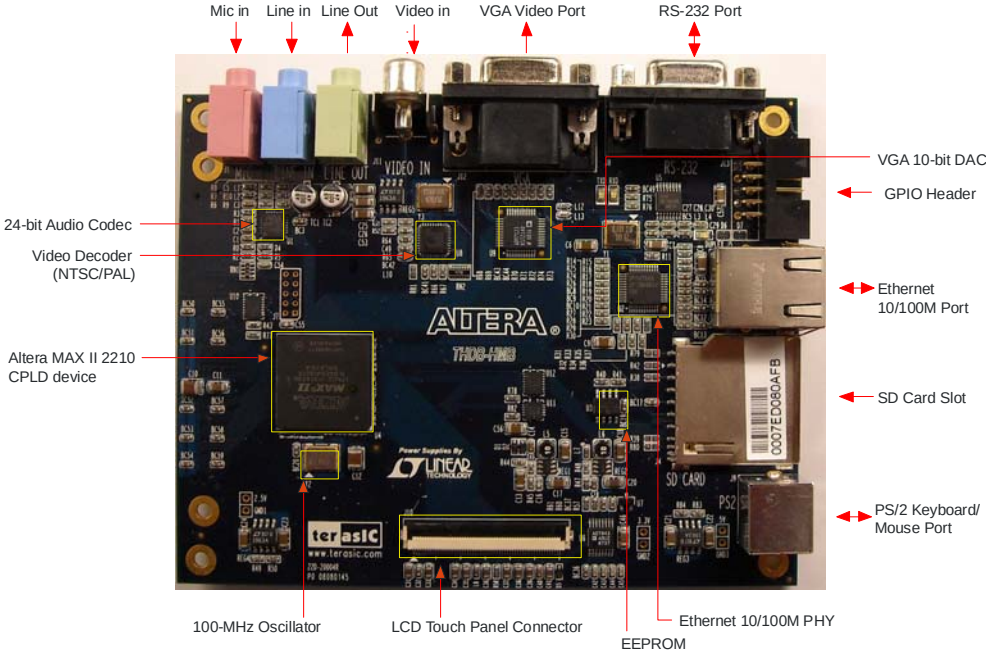
- MAX II CPLD used for
  - Time-division multiplexing of signals
  - Voltage level shifting
- Interfaces
  - HSMC expansion interface
  - Audio codec interface
  - Video decoder interface
  - SD-Card Flash interface
  - VGA interface
  - Serial interface
  - PS/2 interface
  - Ethernet
- Clocking circuitry
- GPIO (version 2.0)
- Memory
- Power supply

Board schematics, board layout database, and assembly files for the LCD Multimedia HSMC v2.0 are included in the board_design_files subdirectory of the installed kit directory.

For information on powering-up the LCD Multimedia HSMC v2.0 and installing the demo software and examples, refer to the user guide provided with your kit.

Figure 2–1 shows the top view of the LCD Multimedia HSMC v2.0.

Figure 2–1. Top View of the LCD Multimedia HSMC v2.0



Notes:
(1) LCD Touch Panel is not shown.

Figure 2–2 shows the back view of the LCD Multimedia HSMC.

Figure 2–2. Back View of the LCD Multimedia HSMC

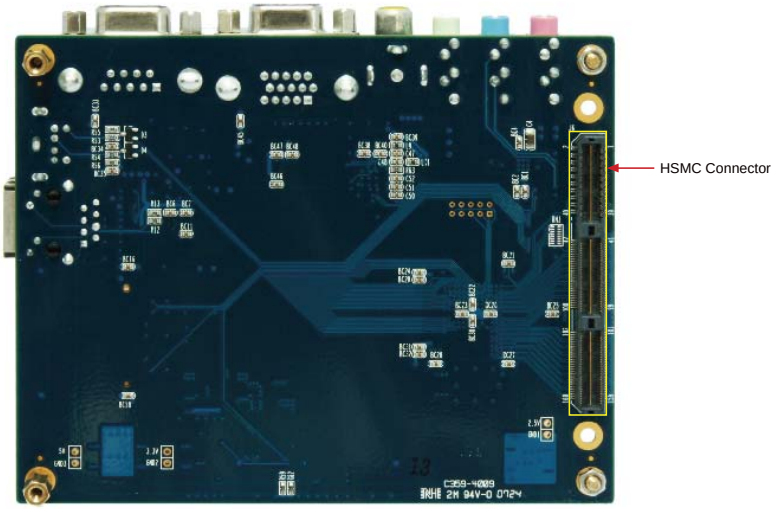


Table 2–1 lists the components and their corresponding board references.

Table 2–1. LCD Multimedia HSMC (Part 1 of 2)

Type	Component/ Interface	Board Reference	Description	Page
Interface Device				
CPLD	MAX II	U4	EPM2210F324C4, 272-pin FineLine BGA 324-pin package	2–5
Level Translator				
I/O	Bidirectional Level Shift Interface	U10, U11, U12	Texas Instruments Bi-Directional Voltage Translators	2–8
Display				
I/O	LCD Touch Screen Display	J10 +Touchscreen, U6	FPC 60B connector	2–16
Connections & Interfaces				
Input	MIC In	J1, U1	Microphone in jack	2–21

Table 2–1. LCD Multimedia HSMC (Part 2 of 2)

Type	Component/ Interface	Board Reference	Description	Page
Input	Line In	J2, U1	24 bit CD quality audio CODEC	2–21
Output	Line Out	J3, U1	24 bit CD quality audio CODEC	2–21
Input	SD Card Socket	J4	128 MB Memory Card	2–23
I/O	Ethernet	J5, U2	10/100 Ethernet PHY/MAC controller	2–25
I/O	RS 232	J8, U5	9 pin connector and transceiver	2–27
I/O	PS/2	J9	5 pin connector, mouse/ keyboard connector	2–28
I/O	GPIO	J13	General Purpose I/O Connector (Mode 1 and 2)	2–29
Input	Video Decoder	J11	RCA jack	2–31
Output	VGA	J12, U9	One VGA output connector (DB15), and 10-bit VGA DAC	2–34
Clock Circuitry				
Oscillator	Clock	Y1, Y2, Y3	Various clock oscillators used for system clock or other dedicated devices.	2–38
Power Supply				
Power Supplies	Analog/Digital Power	Reg1, Reg2, Reg3, Reg4, Reg5	Switching and linear regulators used for powering analog and digital components.	2–39
EEPROM				
Memory	I2C EEPROM	U3	Uses one 2K bit EEPROM.	2–40
Expansion Interface				
I/O	HSMC	J6	Expansion connector used to interface with Altera starter and development boards	2–42

Interface Device

MAX II CPLD-EPM2210F324 (U4)

The LCD Multimedia HSMC uses the MAX II 2210 CPLD EPM2210F324C3 device (U4). Table 2–2 lists MAX II CPLD board reference and manufacturing information.

Table 2–2. MAX II CPLD Manufacturing Information

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
U4	MAX II CPLD for TDM and level shifting/buffering	Altera	EPM2210F324C3N	www.altera.com

The primary functions for this device are to

1. Provide time-division multiplexing (TDM) functions to the LCD and VGA color data bus.
2. Provide level shifting feature for the 2.5V input (Cyclone III FPGA) and 3.3V required by many of the interface chips.

This package has 272 user I/Os and comes in a 324-pin Fine-Line BGA package. Table 2–3 lists Max II device features.

Table 2–3. Max II Device Features

Architectural Feature	Results
Altera's second generation low-cost CPLDs	• Low cost packaging • Large number of logic elements • LUT based architecture • Fastest CPLD supports up to 300MHz clock frequency
Lowest power consumption CPLD	• Power down capability that conserves the battery life • Lowest dynamic power • Hot-socketing support • Single power supply simplicity
On-chip user Flash memory	• 8kbit user accessible flash memory • Enables the integration of discrete and non-volatile storage reducing chip count and cost

Table 2–3. Max II Device Features	
Architectural Feature	**Results**
Real time In-signal programmability	• Capable of downloading a second design while the device is operational
I/O capabilities	• Supports interfacing with 1.8V, 2.5V and 3.3V logic levels of the device due to Multivolt I/O capability • Schmitt triggers, programmable slew rate & programmable drive strength improve signal integrity

Table 2–4 lists the Max II EPM2210F324C4 device pin count.

Table 2–4. Max II Device Pin Count	
Board Component	**Pins**
SD Card	6
Ethernet	18
Audio Codec	6
RS232 and PS/2	4
LCD Touch Panel	38
Video Decoder	14
VGA	25
MAX II CPLD ISP	4
HSMC(1)	88
Total Pins Used	203
Total EPM2210F324C4 User I/Os	272
Unused pins	69

Note to Table 2–4:
(1) The HSMC pins include all pins between the FPGA and the MAX II CPLD

For additional information about Altera devices, go to **www.altera.com/products/devices**.

Block Diagram of bus-controller logic in the MAX II CPLD

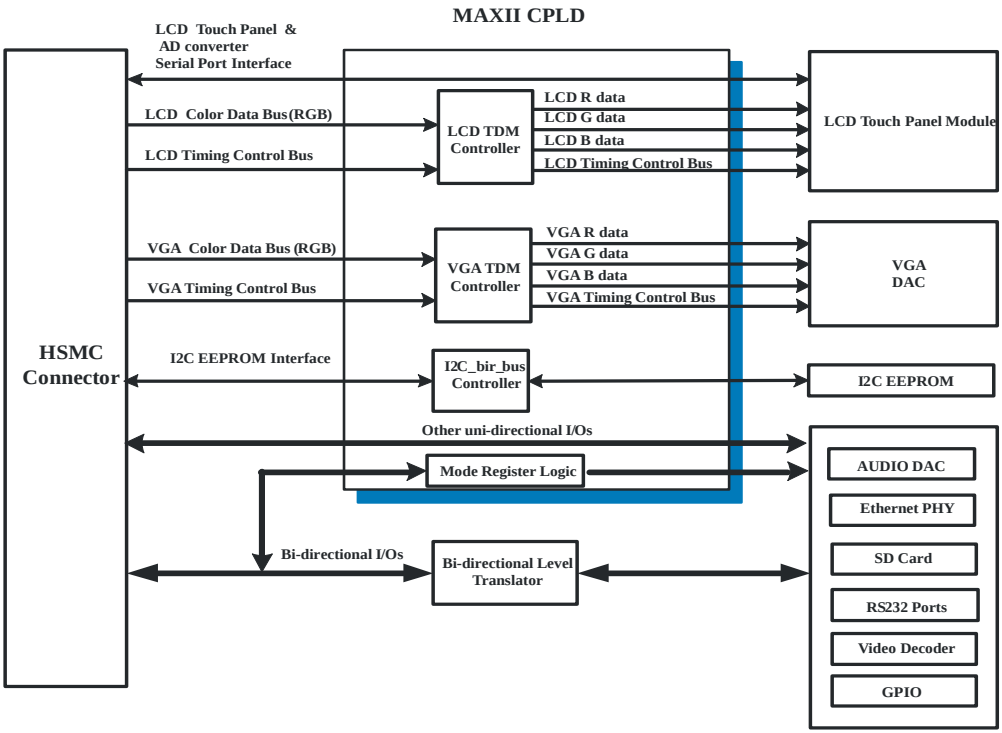
Figures 2–3 shows the block diagram of Bus Controller logic in the MAX II device. Both the LCD TDM block is a simple 8-bit to 24-bit data de-multiplexing function which drives the LCD panel. Similarly, the VGA TDM block is a 10bit to 30bit data de-multiplexing function which

drives the VGA DAC. In the LCD TDM block, the 8-bit input data (successive BGR color data) comes in at 3x the rate of the 24-bit output data bus (8-bit B + 8bit G + 8bit R).

The purpose of adding this complexity to the design of the LCD Multimedia HSMC was to allow for more functionality given the constraint of a pin-limited HSMC connector interface.

The I2CBir_bus block provides birdirectional control for I2C Serial EEPROM data bus. All other signals that pass through the MAXII device are uni-directional and are simply buffered and level-shifted in the MAX II.

Figure 2–3. The Block Diagram of MAX II Bus Controller (Mode 0)



Level Translators and MAX II Mode Control Register

Bidirectional level shift interface (U10, U11, U12)

There are 3 bidirectional level shifters on the board (U10, U11, and U12). These chips are all Texas Instruments TXB0108 or TXB0104 devices. U10 is used completely as bi-directional level-shifters from 2.5V input (Cyclone III FPGA) to 3.3V required by many of the interface chips. U11 and U12, however, are also used to multiplex signals based on the setting of the mode-select logic register. Table 2–5 lists bidirectional level shift interface reference and manufacturing information.

Table 2–5. Bidirectional Level Shift Interface Manufacturing Information

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
U11	4-Bit Bidirectional Voltage Level Translator with Auto-Direction Sensing	Texas Instruments	TXB0104	www.ti.com
U10, U12	8-Bit Bidirectional Voltage Level Translator with Auto-Direction Sensing	Texas Instruments	TXB0108	www.ti.com

Figure 2–4 shows the block diagram and signals for the combination of the HSMC connector, the MAX II device and the level-shifters.

Figure 2–4. Block Diagram of Bidirectional Level Shift Interface and MAX II Control

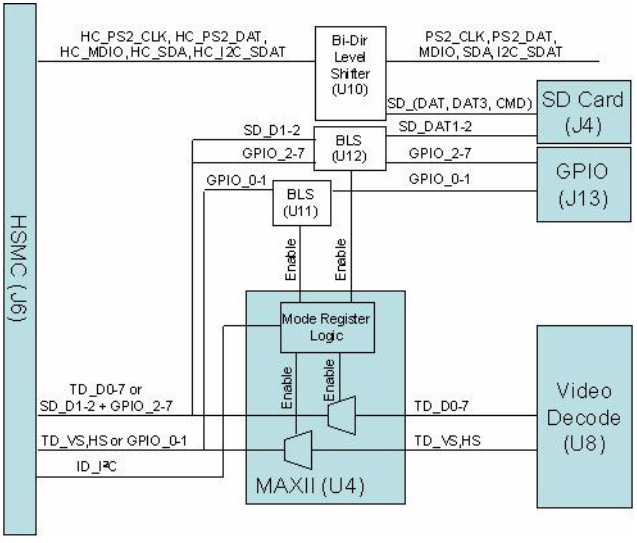


Figure 2–5 shows the Level Shift Interface schmeatic.

Figure 2–5. Level Shift Interface Schematic

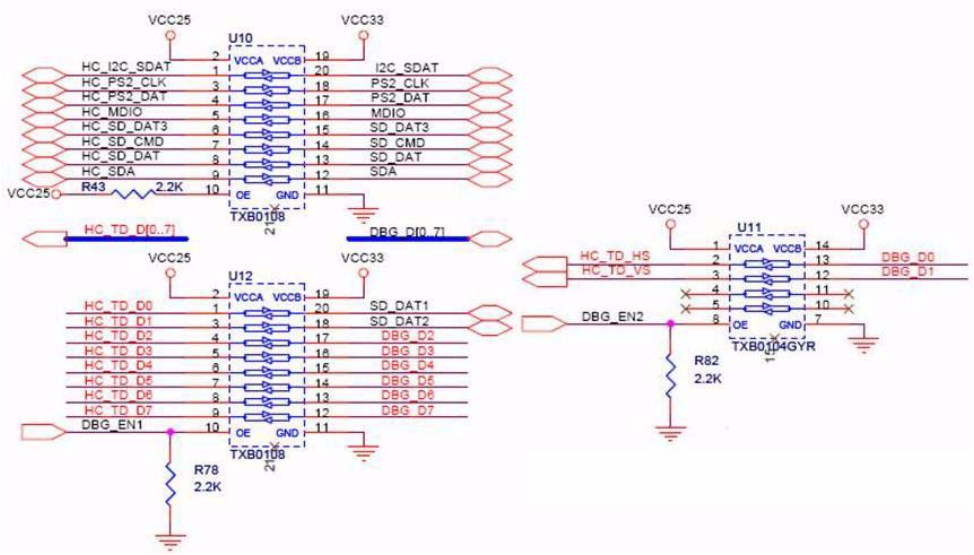


Table 2–6 shows the pinouts of level shift interface with HSMC connector for U11 (straight level shifting).

Table 2–6. Device U11 Level Shift Interface Pinouts with HSMC Connector

	Signal Name		Interface Device	
HSMC Pin #	HSMC Side	Device Side	Pin #	Signal Description
33	HC_I2C_SDAT	I2C_SDAT	U1.27,U8.33	I2C data to audio codec and video decoder.
43	HC_PS2_CLK	PS2_CLK	J9.6	PS/2 Clock
47	HC_PS2_DAT	PS2_DAT	J9.1	PS/2 Data
49	HC_MDIO	MDIO	U2.30	Ethernet PHY Management Data I/O
53	HC_SD_DAT3	SD_DAT3	J4.1	SD 1-bit Mode: Card Detect SD 4-bit Mode: Data3 SPI Mode: Chip Select (Active Low)

Table 2–6. Device U11 Level Shift Interface Pinouts with HSMC Connector

	Signal Name		Interface Device	
HSMC Pin #	HSMC Side	Device Side	Pin #	Signal Description
44	HC_SD_CMD	SD_CMD	J4.2	SD 1-bit Mode: Command Line SD 4-bit Mode: Command Line SPI Mode: Data In
48	HC_SD_DAT	SD_DAT	J4.7	SD 1-bit Mode: Data Line SD 4-bit Mode: Data0 SPI Mode: Data Out
50	HC_SDA	SDA	J10.44	LCD 3-Wire Serial Interface Data

Bidirectional level shift interfaces and the Mode Control Registers

In order to provide additional peripheral flexibility, the LCD Multimedia HSMC v2.0 provides the user with 3 separate pinout modes. These modes as described in Table 2–7, affect the usage of the Video Decoder (U8), the SD-Card Connector (J4), and the 10-pin GPIO connector (J13). This section describes the mode configuration details and signals that are affected for each mode. Appendix C describes the EEPROM and Mode-Settings tool used to change the mode register value.

Table 2–7. Mode Control Register Settings and Actions

Mode Register	Action	Video Decoder	GPIO	SD Card
0	Video decoder in standard x8 operating mode. SD-Card in 1-bit mode. No GPIO.	Enabled	0	1-bit
1	Video decoder disabled. 8 GPIO available. SD-Card in 4-bit mode.	Disabled	8	4-bit
2	Video decoder enabled, but Vertical Sync (VS) and Horizontal Sync (HS) pins disabled. 2 GPIO pins available - others are disabled. SD-Card in 1-bit mode.	Enabled but no VS or HS signals	2	1-bit

Bidirectional level shift interfaces for Mode 0

Mode 0 is the **compatibility mode** for the original version of the LCD Multimedia HSMC. In this mode, The bidirectional voltage level shifters U11 and U12 are disabled, and the SD-Card (J4) has a 1-bit interface, there no GPIO pins available on J13, and the video decoder (U8) is enabled. Figure 2–6 shows the block diagram for this mode which is a subset of the block diagram shown in Figure 2–4.

Figure 2–6. Block Diagram of Bidirectional Level Shift Interface for Mode 0

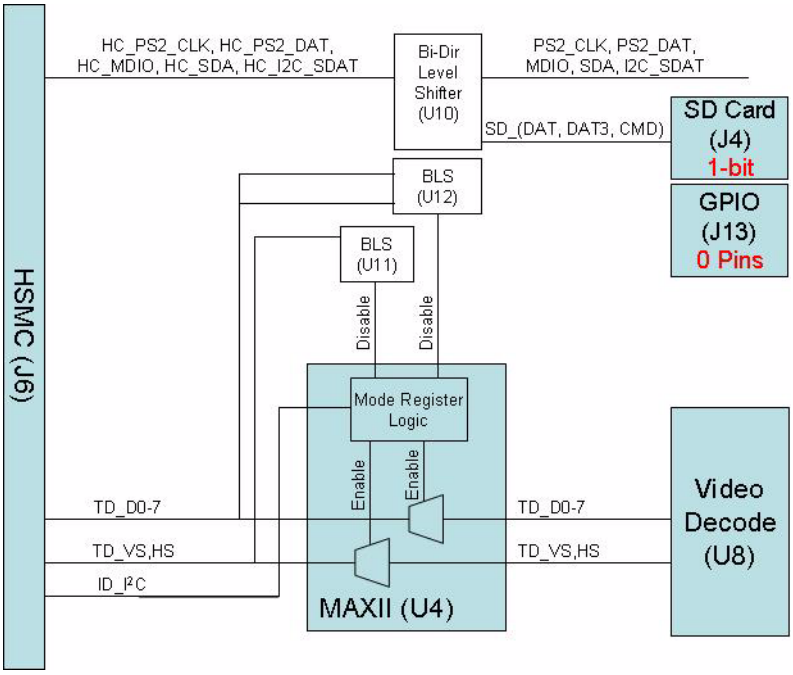


Table 2–8 shows the signals enabled to the HSMC connector.

Table 2–8. MAXII Pinouts with HSMC Connector in Mode 0

	Signal Name		Interface Device	
HSMC Pin #	HSMC Side	Device Side	Pin #	Signal Description
56	HC_TD_D0	TD_D0	U4.V8	Video decoder data0
60	HC_TD_D1	TD_D1	U4.T8	Video decoder data1
62	HC_TD_D2	TD_D2	U4.T9	Video decoder data2
66	HC_TD_D3	TD_D3	U4.V9	Video decoder data3
68	HC_TD_D4	TD_D4	U4.U9	Video decoder data4
72	HC_TD_D5	TD_D5	U4.U10	Video decoder data5
74	HC_TD_D6	TD_D6	U4.V10	Video decoder data6
78	HC_TD_D7	TD_D7	U4.T10	Video decoder data7

Table 2–8. MAXII Pinouts with HSMC Connector in Mode 0

	Signal Name		Interface Device	
HSMC Pin #	HSMC Side	Device Side	Pin #	Signal Description
84	HC_TD_VS	TD_VS	U4.V11	Video decoder vertical sync signal
86	HC_TD_HS	TD_HS	U4.T11	Video decoder horizontal sync signal

Note:
(1) * Bidirectional Voltage Level Shifters U11 and U12 are disabled in this mode

Bidirectional level shift interfaces for Mode 1

In mode 1, the bidirectional voltage level shifters U11 and U12 are enabled and the multiplexing in the MAXII device is disabled. This mode disables the signals from the video decoder (U8) and provides the signals to all the SD-Card (J4) to run in 4-bit mode. Also there are now 8 GPIO pins available on J13. Figure 2–7 shows the block diagram for this mode which is a subset of the block diagram shown in Figure 2–4.

Figure 2–7. Block Diagram of Bidirectional Level Shift Interface for Mode 1

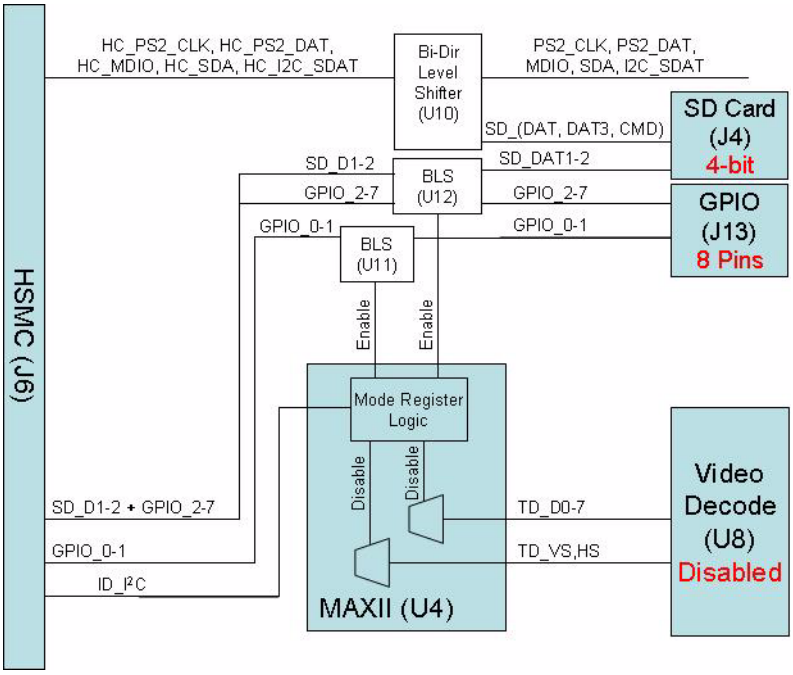


Table 2–9 shows the signals enabled to the HSMC connector.

Table 2–9. Device U11 and U12 Level Shift Interface Pinouts with HSMC Connector in Mode 1

	Signal Name		Interface Device	
HSMC Pin #	HSMC Side	Device Side	Pin #	Signal Description
56	HC_TD_D0	SD_DAT1	U12.20	SD-Card data bus signal 1 for 4-bit mode
60	HC_TD_D1	SD_DAT2	U12.18	SD-Card data bus signal 2 for 4-bit mode
62	HC_TD_D2	DBG_D2	U12.17	GPIO data pin 2
66	HC_TD_D3	DBG_D3	U12.16	GPIO data pin 3
68	HC_TD_D4	DBG_D4	U12.15	GPIO data pin 4
72	HC_TD_D5	DBG_D5	U12.14	GPIO data pin 5
74	HC_TD_D6	DBG_D6	U12.13	GPIO data pin 6
78	HC_TD_D7	DBG_D7	U12.12	GPIO data pin 7

Table 2–9. Device U11 and U12 Level Shift Interface Pinouts with HSMC Connector in Mode 1

	Signal Name		Interface Device	
HSMC Pin #	HSMC Side	Device Side	Pin #	Signal Description
84	HC_TD_VS	DBG_D1	U11.12	GPIO data pin 1
86	HC_TD_HS	DBG_D0	U11.13	GPIO data pin 0

Note:
(1) * Multiplexers in the MAX II device are disabled in this mode.

Bidirectional level shift interfaces for Mode 2

In mode 2, the bidirectional voltage level shifter U11 is enabled, allowing GPIO signals 0 and 1 to propagate to the GPIO Header (J13). The complementary multiplexer in the MAX II device disables the vertical sync and horizontal sync signals from the video decoder chip (U8) from propagating. Also in this mode U12 is disabled thus GPIO signals 2 – 7 are not available on the GPIO header (J13), but the complementary multiplexer in the MAX II device enables the propagation of the data bus signals 0 – 7 from the video decoder (U8) to the HSMC connector (J6). Figure 2–8 shows the block diagram for this mode which is a subset of the block diagram shown in Figure 2–4.

Figure 2–8. Block Diagram of Bidirectional Level Shift Interface for Mode2

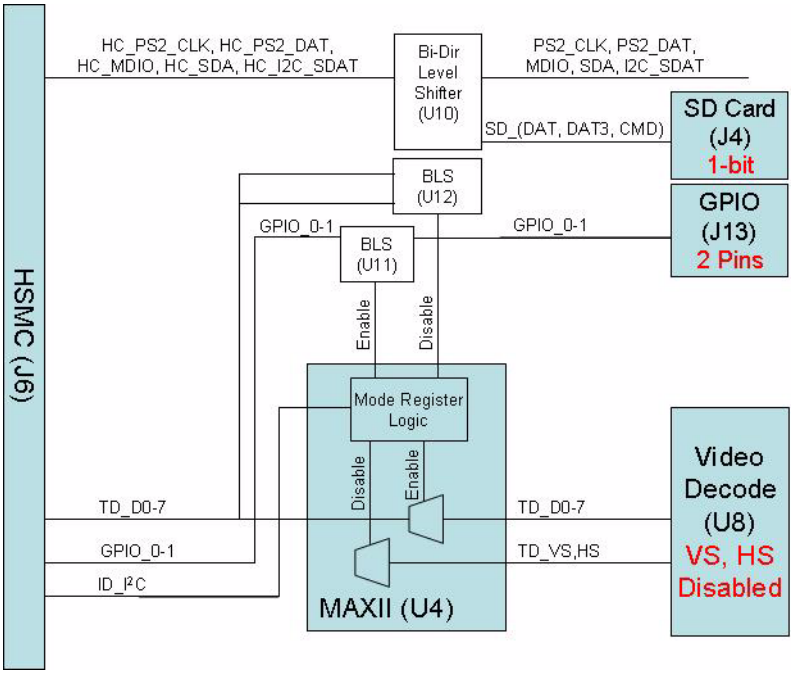


Table 2–10 shows the signals enabled to the HSMC connector.

Table 2–10. MAX II and U11 Device Pinouts with HSMC Connector in Mode 2

	Signal Name		Interface Device	
HSMC Pin #	HSMC Side	Device Side	Pin #	Signal Description
56	HC_TD_D0	TD_D0	U4.V8	Video decoder data0
60	HC_TD_D1	TD_D1	U4.T8	Video decoder data1
62	HC_TD_D2	TD_D2	U4.T9	Video decoder data2
66	HC_TD_D3	TD_D3	U4.V9	Video decoder data3
68	HC_TD_D4	TD_D4	U4.U9	Video decoder data4
72	HC_TD_D5	TD_D5	U4.U10	Video decoder data5
74	HC_TD_D6	TD_D6	U4.V10	Video decoder data6
78	HC_TD_D7	TD_D7	U4.T10	Video decoder data7

Table 2–10. MAX II and U11 Device Pinouts with HSMC Connector in Mode 2				
	Signal Name		Interface Device	
HSMC Pin #	HSMC Side	Device Side	Pin #	Signal Description
84	HC_TD_VS	DBG_D1	U11.12	GPIO data pin 1
86	HC_TD_HS	DBG_D0	U11.13	GPIO data pin 0

Note:
(1) * Bidirectional Voltage Level Shifter U12 is disabled in this mode. Vertical and horizontal sync signals from the video decoder (U8) are disabled via the MAX II device in this mode

Display

LCD Touch Panel Display

The board provides a 4.3" Toppoly TD043MTEA1 active matrix color display, with 800x480 pixel resolution. Table 2–11 lists LCD Touch Panel Display board reference and manufacturing information.

Table 2–11. LCD Touch Panel Display Manufacturing Information				
Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
Display + J10	4.3" Active Matrix Color LCD Screen (480x800 RGB) + Touch Panel	Toppoly	TD043MTEA1	www.toppoly.com
U6	12-Bit ADC for resistive touchscreen sensing	Analog Devices	AD7843	www.analog.com

The LCD panel supports the 24-bit parallel RGB data interface and provides a 3-wire interface to control the display function registers. The LCD Multimedia HSMC is also equipped with an Analog Devices AD7843 touch screen digitizer chip. The AD7843 is a 12-bit analog to digital converter (ADC) for digitizing x and y coordinates of touch points applied to the touch screen.

Timing Protocol of the LCD TDM Controller

Figure 2–9 below describes the input timing waveform information of the LCD TDM Controller implemented in the MAX II CPLD. The 8-bit wide HC_LCD_DATA signal is presumed to contain a stream of color pixel data, with each pixel represented by three successive clock-cycles of the stream. The data is presented in the order "BGR". The LCD TDM

Controller uses the HC_HD pulse to determine the position of the BLUE color sample, and thus the start of each three-clock pixel-period. State transitions on HC_HD (0 →1 or 1 →0) coincide with the presentation of BLUE color on the HC_LCD_DATA input. The GREEN and RED values for that same pixel are presented on the next two clock-cycles. Figure 2–10 shows the timing information on the output side. The LCD TDM block will generate an output NCLK clock and 24-bit RGB data to the LCD panel. The NCLK signal runs at 1/3 the frequency of the incoming clock HC_NCLK.

Figure 2–9. The Timing Diagram On the Input Side of VGA TDM Controller

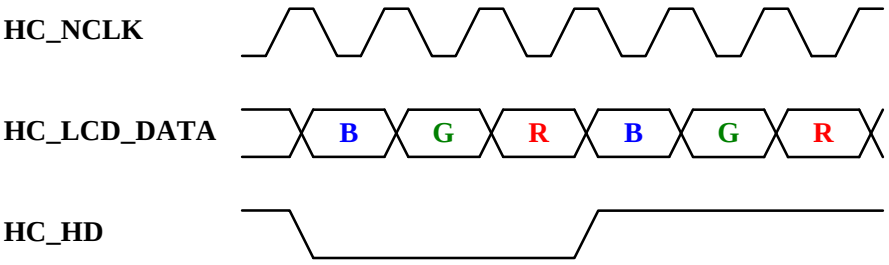
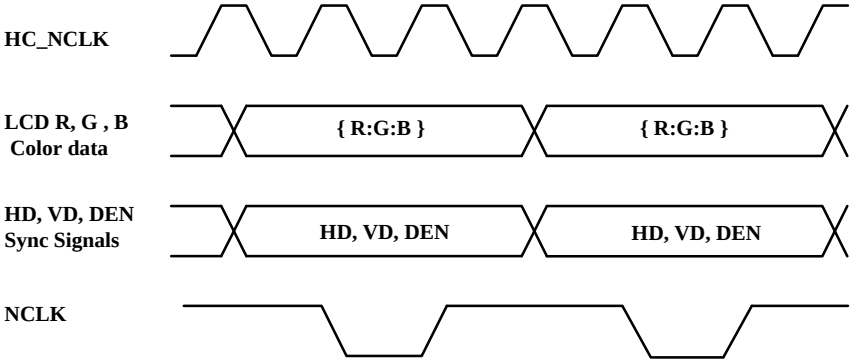


Figure 2–10. The Timing Diagram On the Output Side of VGA TDM Controller



The pin assignments are listed in Tables 2–12

Tables 2–12 shows the pinout of LCD Touch Panel with HSMC connector.

Table 2–12. LCD Touch Panel Pinout with HSMC Connector

HSMC Connector		MAX II		LCD Touch Panel		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_VD	132	D14	F6	VD	6	LCD Vertical Sync Input
HC_HD	134	C14	F5	HD	7	LCD Horizontal Sync Input
HC_DEN	138	C15	E5	DEN	8	LCD RGB Data Enable
HC_NCLK	95	K13	E4	NCLK	9	LCD Clock
HC_LCD_DATA[0]	145	D17	H1	R[0]	28	LCD red data bus bit 0
			E3	G[0]	19	LCD green data bus bit 0
			D4	B[0]	10	LCD blue data bus bit 0
HC_LCD_DATA[1]	149	C17	H2	R[1]	29	LCD red data bus bit 1
			F3	G[1]	20	LCD green data bus bit 1
			C3	B[1]	11	LCD blue data bus bit 1
HC_LCD_DATA[2]	151	C16	J2	R[2]	30	LCD red data bus bit 2
			F1	G[2]	21	LCD green data bus bit 2
			C2	B[2]	12	LCD blue data bus bit 2
HC_LCD_DATA[3]	126	D13	J1	R[3]	31	LCD red data bus bit 3
			F2	G[3]	22	LCD green data bus bit 3
			D3	B[3]	13	LCD blue data bus bit 3
HC_LCD_DATA[4]	128	D15	J3	R[4]	32	LCD red data bus bit 4
			G2	G[4]	23	LCD green data bus bit 4
			D1	B[4]	14	LCD blue data bus bit 4
HC_LCD_DATA[5]	146	B15	K3	R[5]	33	LCD red data bus bit 5
			G1	G[5]	24	LCD green data bus bit 5
			D2	B[5]	15	LCD blue data bus bit 5
HC_LCD_DATA[6]	150	B14	K1	R[6]	34	LCD red data bus bit 6
			G3	G[6]	25	LCD green data bus bit 6
			E2	B[6]	16	LCD blue data bus bit 6
HC_LCD_DATA[7]	152	A15	K2	R[7]	35	LCD red data bus bit 7
			H3	G[7]	26	LCD green data bus bit 7
			E1	B[7]	17	LCD blue data bus bit 7

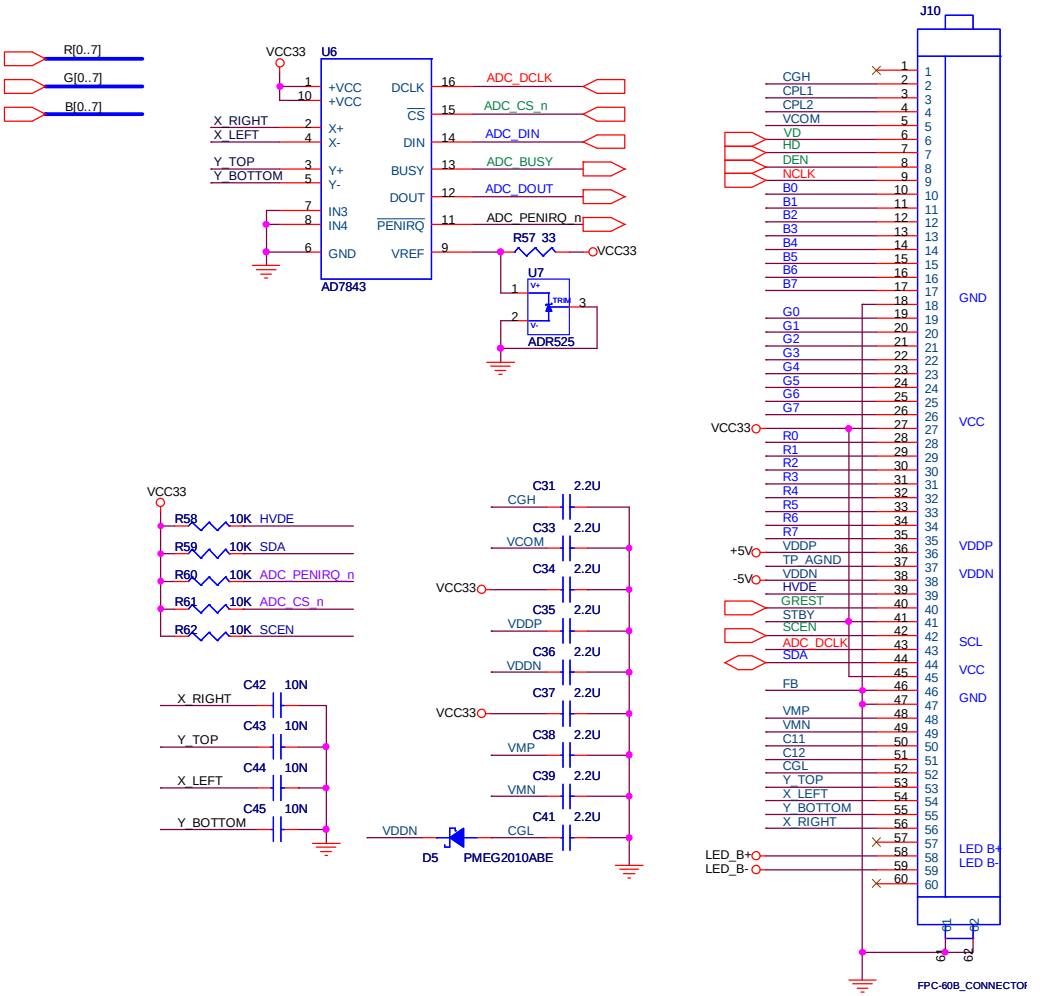
Table 2–12. LCD Touch Panel Pinout with HSMC Connector

HSMC Connector		MAX II		LCD Touch Panel		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_GREST	140	C13	L2	GREST	40	LCD Global Reset, Low Active
HC_SCEN	144	B13	L1	SCEN	42	LCD 3-Wire Serial Interface Enable
HC_SDA	50	U11-5(1)	U11-10(1)	SDA	J10.44	LCD 3-Wire Serial Interface Data
HC_ADC_DCLK	157	B18	L3	ADC_DCLK	U6.16	AD7843/LCD 3-Wire Serial Interface Clock
HC_ADC_DIN	155	B16	N2	ADC_DIN	U6.14	AD7843 Serial Interface Data In
HC_ADC_CS_n	143	D18	N1	ADC_CS_n	U6.15	AD7843 Serial Interface Chip Select Input
HC_ADC_DOUT	122	E13	M1	ADC_DOUT	U6.12	AD7843 Serial Interface Data Out
HC_ADC_PENIRQ_n	156	A14	M3	ADC_PENIRQ_n	U6.11	AD7843 pen Interrupt
HC_ADC_BUSY	120	E15	M2	ADC_BUSY	U6.13	AD7843 Serial Interface Busy

Notes to Table 2–12:
(1) These signals do not go through the MAX II chip. They pass through the MAX3378 level translator chip, U11.

Figure 2–11 shows the LCD Touch Panel schematic.

Figure 2–11. LCD Touch Panel Schematic



Interfaces/ Connectors

This section describes the following LCD Multimedia HSMC's interface/connector blocks:

- Audio Codec Interface (J1, J2, J3)
- SD Card socket (J4)
- Ethernet connector (J5)
- RS 232 connector (J8)
- UART and PS/2 connector (J9)
- Video Decoder connector (J11)
- VGA DAC connector (J12)

Audio Codec Interface

The board provides 24-bit CD-Quality audio via the Wolfson WM8731 audio CODEC (enCODer/DECoder). Table 2–13 lists Audio Codec Interface board reference and manufacturing information.

Table 2–13. Audio Codec Interface Manufacturing Information

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
U1	CD quality, low power, high quality audio codec.	Wolfson Microelectronics	WM8731	www.wolfsonmicro.com

The Audio Codec Interface features:

- 24-bit sigma-delta audio CODEC
- Line-level input, line-level output, and microphone input jacks
- Sampling frequency: 8 to 96 KHz

This chip supports microphone-in (J1), audio-in (J2), and audio-out (J3) ports, with a sample rate adjustable from 8 kHz to 96 kHz. The WM8731 is controlled by a serial I2C bus interface, which is connected to pins on the HSMC connector.

Tables 2–14 shows the pinout of Audio Codec with HSMC connector.

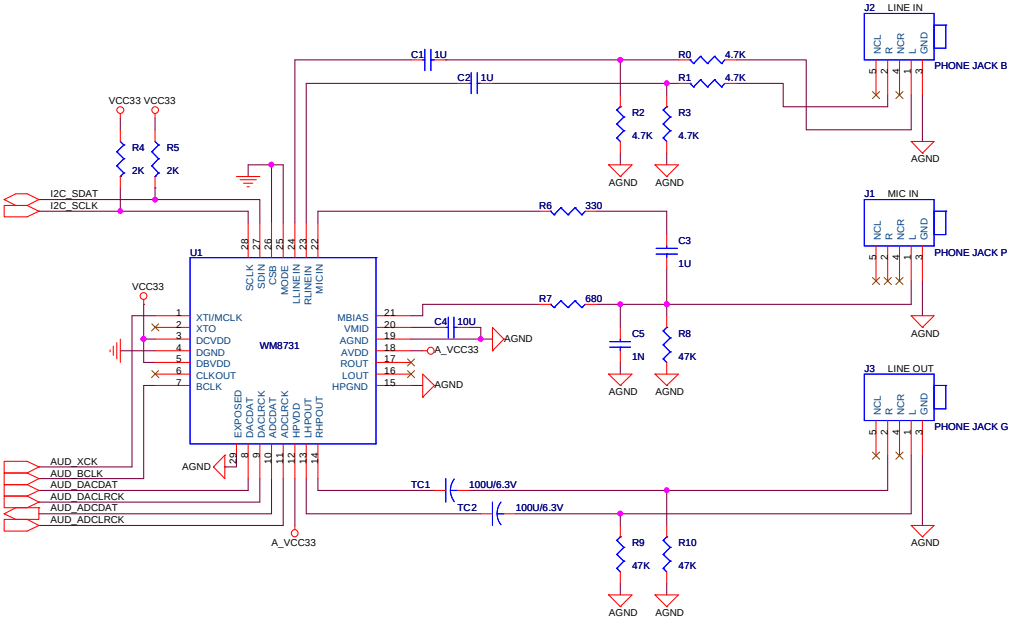
Table 2–14. Audio Codec Pinout with HSMC Connector

HSMC Connector		MAX II		Audio Codec		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_AUD_BCLK	113	G17	U13	AUD_BCLK	7	Audio CODEC Bit-Stream Clock
HC_AUD_XCK	39	T16	U14	AUD_XCK	1	Audio CODEC Chip Clock
HC_AUD_DACDAT	109	H17	V13	AUD_DACDAT	8	Audio CODEC DAC Data
HC_AUD_DACLRCK	107	H18	T13	AUD_DACLRCK	9	Audio CODEC DAC LR Clock
HC_AUD_ADCDAT	40	R15	T12	AUD_ADCDAT	10	Audio CODEC ADC Data
HC_AUD_ADCLRCK	103	H16	V12	AUD_ADCLRCK	11	Audio CODEC ADC LR Clock
HC_I2C_SDAT	33	U10-2(1)	U10-13(1)	I2C_SDAT	27	I2C Data
HC_I2C_SCLK	34	P15	U11	I2C_SCLK	28	I2C Clock

Note:
(1) These signals do not go through the MAX II chip. They pass through the MAX3378 level translator chip, U10.
(2) Default, the audio chip is configured as a SLAVE mode.

Figure 2–12 shows the Audio Codec connector schematic.

Figure 2–12. Audio Codec Connector Schematic



SD Card

The board includes a SD Card socket and provides SPI mode for SD Card access. It can be accessible as memory in both SPI and and 1-bit SD mode. The SD-Card can also be accessed in 4-bit mode when the Mode Control Register in the MAX II Device is set to 1 (see "Level Translators and MAX II Mode Control Register" and Appendix C).

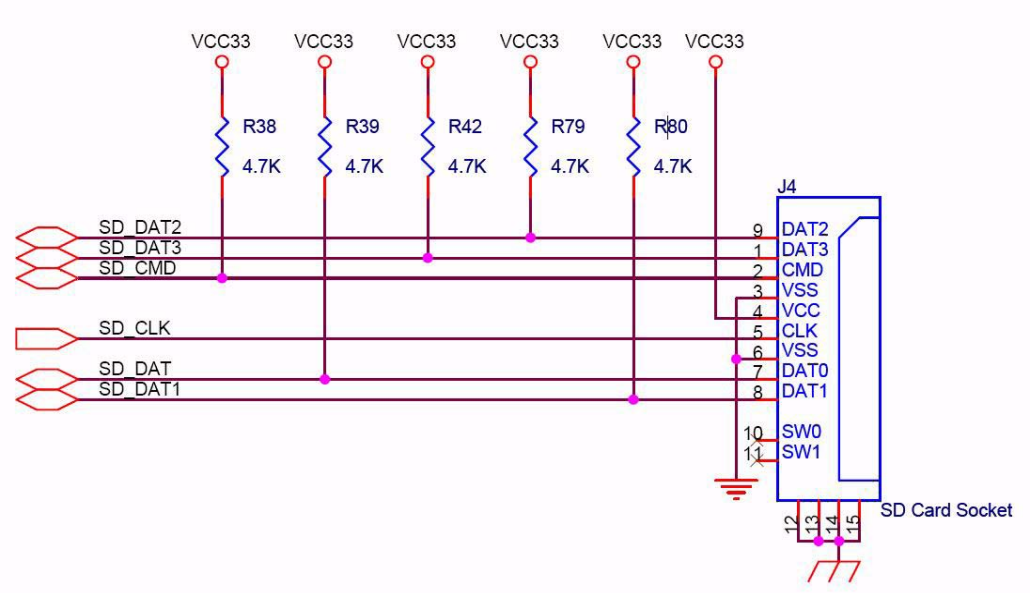
Tables 2–15 shows the pinout of SD Card Socket with HSMC connector.

Table 2–15. SD Card Pinout with HSMC Connector

HSMC Connector		Switch Pin #s		SD Card		
Pin No.	Signal Name	HSMC Side	Device Side	Signal Name	Pin No.	Description
53	HC_SD_DAT3	U10.6	J4.1	SD_DAT3	J4.1	SD 1-bit Mode: Card Detect SD 4-bit Mode: Data3 SPI Mode: Chip Select (Active Low)
44	HC_SD_CMD	U10.7	J4.2	SD_CMD	J4.2	SD 1-bit Mode: Command Line SD 4-bit Mode: Command Line SPI Mode: Data In
101	HC_SD_CLK	U4.J16	U4.P1	SD_CLK	J4.5	Clock
48	HC_SD_DAT	U10.8	J4.7	SD_DAT	J4.7	SD 1-bit Mode: Data Line SD 4-bit Mode: Data0 SPI Mode: Data Out
56	HC_TD_D0	U12.1	U12.20	SD_DAT1	J4.8	SD 4-bit: Data1 (MAXII Mode Control Register = 1)
60	HC_TD_D1	U12.3	U12.18	SD_DAT2	J4.9	SD 4-bit: Data2 (MAXII Mode Control Register = 1)

Figure 2–13 shows the SD Card interface schematic.

Figure 2–13. SD Card Interface Schematic



Ethernet PHY

Ethernet support is provided via the National Semiconductor DP83848C Ethernet Physical Layer Transceiver chip and an RJ-45 connector (J5). Table 2–16 lists Ethernet PHY board reference and manufacturing information.

Table 2–16. Ethernet PHY Manufacturing Information

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
U2	Single Port 10/100 Mb/s Ethernet Physical Layer Transceiver	National Semiconductor	DP83848C	www.national.com

The DP83848C device has the following features:

- Single Port 10/100 Mb/s Ethernet Physical Layer Transceiver

- Supports both 100Base-T and 10Base-T Ethernet protocols
- Supports Auto-MDIX for 10/100 Mb/s

The DP83848C is one port Fast Ethernet PHY Transceivers supporting IEEE 802.3 physical layer applications at 10 Mbps and 100 Mbps. The DP83848C provides Media Independent Interface (MII) to connect DP83848C to a MAC in the FPGA.

Tables 2–17 shows the pinout of Ethernet PHY with HSMC connector.

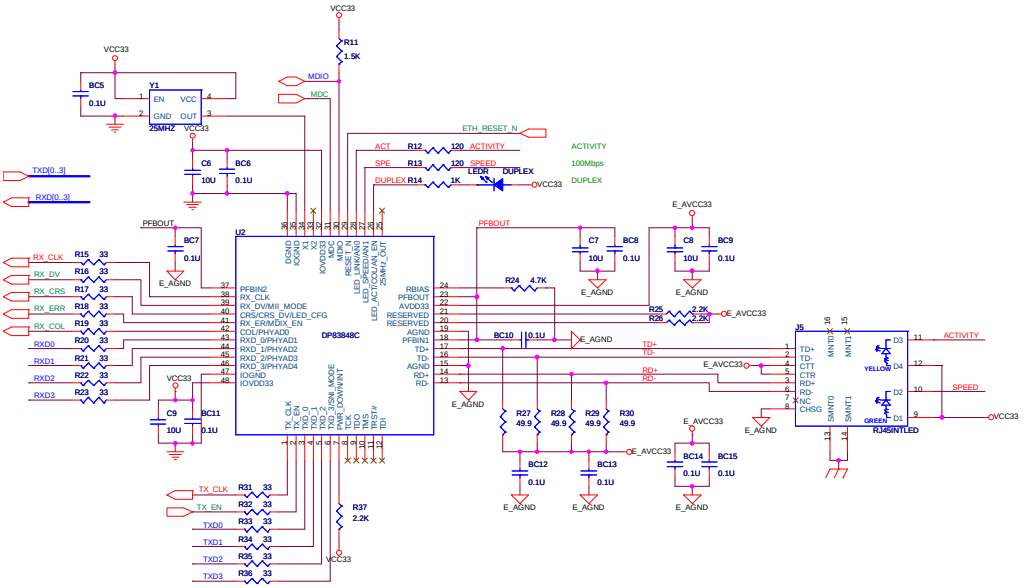
Table 2–17. Ethernet PHY Pinout with HSMC Connector

HSMC Connector		MAX II		Ethernet PHY		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_TX_CLK	158	A13	T2	TX_CLK	1	MII Transmit Clock
HC_TX_EN	125	F18	R3	TX_EN	2	MII Transmit Enable
HC_TXD[0]	127	F17	P4	TXD0	3	MII Transmit Data bit 0
HC_TXD[1]	131	E17	R1	TXD1	4	MII Transmit Data bit 1
HC_TXD[2]	133	E18	R2	TXD2	5	MII Transmit Data bit 2
HC_TXD[3]	137	E16	P2	TXD3	6	MII Transmit Data bit 3
HC_ETH_RESET_N	121	F16	T3	Eth_RESET_N	29	DP83848C Reset
HC_MDIO	49	U10.5	U10.16	MDIO	30	Management Data I/O
HC_MDC	139	D16	U1	MDC	31	Management Data Clock
HC_RX_CLK	96	H14	J5	RX_CLK	38	MII Receive Clock
HC_RX_DV	116	E14	H5	RX_DV	39	MII Receive Data valid
HC_RX_CRS	92	H15	H4	RX_CRS	40	MII Carrier Sense
HC_RX_ERR	90	G13	H6	RX_ERR	41	MII Receive Error
HC_RX_COL	114	F14	G6	RX_COL	42	MII Collision Detect
HC_RXD[0]	102	G15	G4	RXD0	43	MII Receive Data bit 0
HC_RXD[1]	104	G12	G5	RXD1	44	MII Receive Data bit 1
HC_RXD[2]	108	F13	G7	RXD2	45	MII Receive Data bit 2
HC_RXD[3]	110	F15	F4	RXD3	46	MII Receive Data bit 3

Notes:
(1) These signals do not go through the MAX II chip. They pass through the TXB0108 level translator chip, U10.

Figure 2–14 shows the Ethernet PHY connector schematic.

Figure 2–14. Ethernet PHY Schematic



RS232 Serial Interface

The board uses the ADM3202 transceiver chip and a 9-pin D-SUB connector for RS-232 communications. Table 2–18 below lists RS 232 Serial Interface board reference and manufacturing information.

Table 2–18. RS232 Serial Interface Manufacturing Information

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
U5	High-Speed, 2-Channel RS232/V.28 Interface Devices	Analog Devices	ADM3202	www.analog.com

Tables 2–19 shows the pinout of RS232 Interface with HSMC connector.

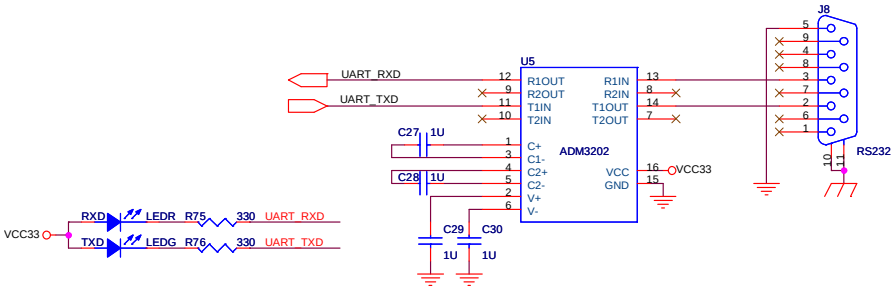
Table 2–19. RS232 Interface Pinout with HSMC Connector

HSMC Connector		MAX II		RS232 Interface		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_UART_RXD	115	G18	K4	UART_RXD	U5-12(1)	UART Receiver
HC_UART_TXD	119	G16	J4	UART_TXD	U5-11(2)	UART Transmitter

Notes:
(1) U5.12 connects to pin 3 on the RS-232 connector (J6) via U5.13.
(2) U5.11 connects to pin 2 on the RS-232 connector (J6) via U5.14.

Figure 2–15 shows the RS232 interface schematic.

Figure 2–15. RS232 Interface Schematic



PS/2 Interface

The LCD Multimedia HSMC includes a standard PS/2 interface and a connector (J9) for a PS/2 keyboard or mouse. The PS/2 interface is a standard interface that is described extensively elsewhere. Implementation of a PS/2 interface can be done either in hardware on the MAXII or FPGA or software in a Nios processor running on the FPGA.

Tables 2–20 shows the pinout of PS/2 Interface with HSMC connector.

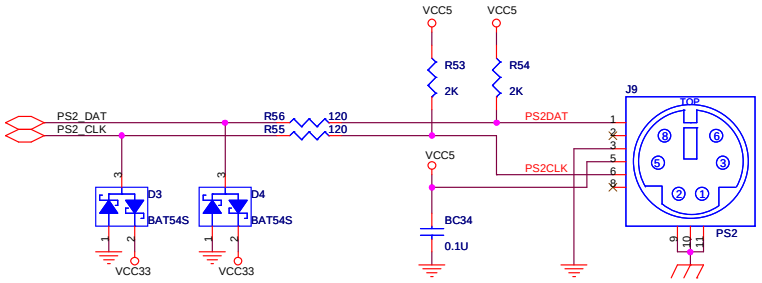
Table 2–20. PS/2 Interface Pinout with HSMC Connector

HSMC Connector		MAX II		*PS/2 Interface*		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_PS2_CLK	43	U10.3	U10.18	PS2_CLK	1	PS/2 Clock
HC_PS2_DAT	47	U10.4	U10.17	PS2_DAT	6	PS/2 Data

Notes:
(1) These signals do not go through the MAX II chip. They pass through the TXB0108 level translator chip, U10.

Figure 2–16 shows the PS/2 interface schematic.

Figure 2–16. PS/2 Interface Schematic



General Purpose I/O Connector (Mode 1 and 2 only)

The LCD Multimedia HSMC v2.0 includes a standard GPIO header (J13). When the Mode Control Register in the MAX II device is set to 1, there are 8 pins available. When it is set to 2, there are two pins available (see "Level Translators and MAX II Mode Control Register" or Appendix C). When the Mode Control Register is set to 0, the GPIO Header pins are disabled.

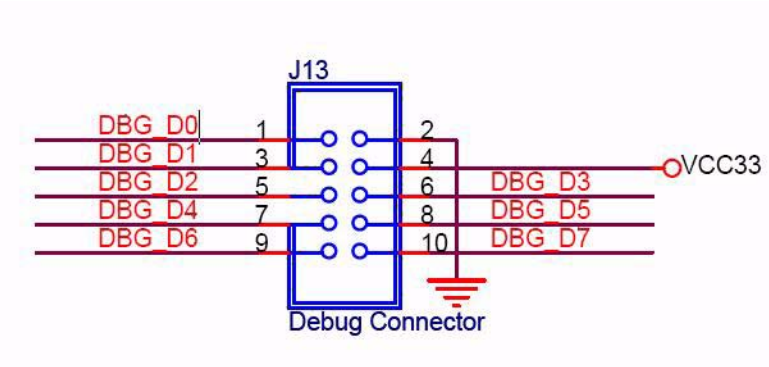
Tables 2–20 shows the pinout of General Purpose I/O Connector (Mode 1 and 2 Only) with HSMC connector.

Table 2–21. General Purpose I/O Connector (Mode 1 and 2 only) Pinouts

HSMC Connector		Switch Pin #s		GPIO Header		Signal Description
Pin No.	Signal Name	HSMC Side	Device Side	Signal Name	Pin No.	
62	HC_TD_D2	U12.4	U12.17	DBG_D2	J13.5	GPIO data pin 2 (Mode Control Register = 1)
66	HC_TD_D3	U12.5	U12.16	DBG_D3	J13.6	GPIO data pin 3 (Mode Control Register = 1)
68	HC_TD_D4	U12.6	U12.15	DBG_D4	J13.7	GPIO data pin 4 (Mode Control Register = 1)
72	HC_TD_D5	U12.7	U12.14	DBG_D5	J13.8	GPIO data pin 5 (Mode Control Register = 1)
74	HC_TD_D6	U12.8	U12.13	DBG_D6	J13.9	GPIO data pin 6 (Mode Control Register = 1)
78	HC_TD_D7	U12.9	U12.12	DBG_D7	J13.10	GPIO data pin 7 (Mode Control Register = 1)
84	HC_TD_VS	U11.3	U11.12	DBG_D1	J13.3	GPIO data pin 1 (Mode Control Register = 1 or 2)
86	HC_TD_HS	U11.2	U11.13	DBG_D0	J13.1	GPIO data pin 0 (Mode Control Register = 1 or 2)

Figure 2–16 shows the General Purpose I/O Connector schematic.

Figure 2–17. General Purpose I/O Connector Schematic



Video Decoder Interface

The board is equipped with an Analog Devices ADV7180 Video decoder chip and RCA input jack (J11). Table 2–22 below lists Video Decoder Interface board reference and manufacturing information.

Table 2–22. Video Decoder Interface

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
U8	10-Bit, 4× Oversampling SDTV Video Decoder	Analog Devices	ADV7180	www.analog.com

The Video Decoder features:

- Multi-format SDTV Video Decoder
- Supports worldwide NTSC/PAL/SECAM color demodulation
- One 10-bit ADC, 4X over-sampling for CVBS
- Supports Composite Video (CVBS) RCA jack input
- Supports digital output formats: 8-bit ITU-R BT.656 YCrCb 4:2:2 output + HS, VS, and FIELD

The ADV7180 is an integrated video decoder that automatically detects and converts a standard analog baseband television signal (NTSC, PAL, and SECAM) into 4:2:2 component video data compatible with 8-bit CCIR601/CCIR656. The ADV7180 is compatible with a broad range of video devices, including DVD players, tape-based sources, broadcast sources, and security/surveillance cameras.

The registers in the Video decoder can be programmed by a serial I2C bus, which is connected to the HSMC connector as indicated in the schematic.

Tables 2–23 shows the pinout of Video Decoder with HSMC connector.

Table 2–23. Video Decoder Pinout with HSMC Connector

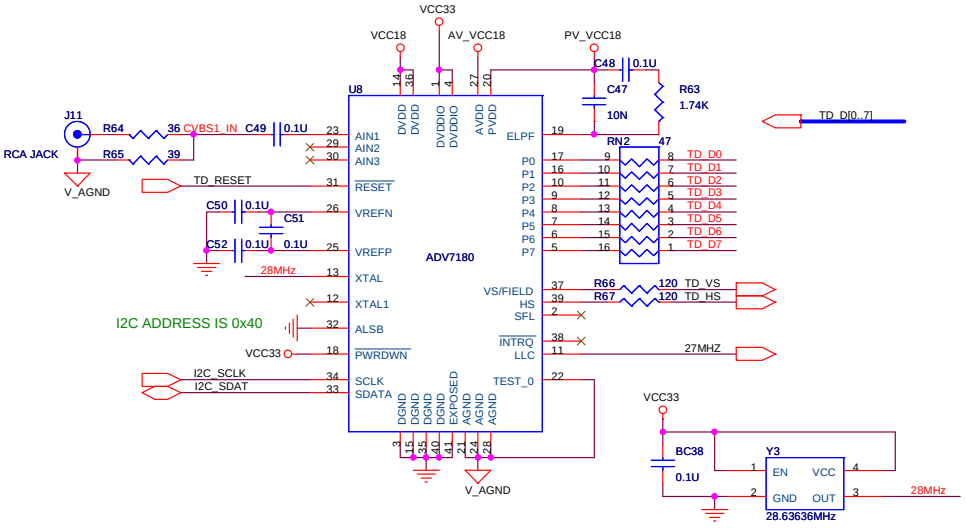
HSMC Connector		MAX II		Video Decoder		
Pin No.	Signal Name	HSMC Side	Device Side	Signal Name	Pin No.	Description
56	HC_TD_D[0]	U4.M15	U4.V8	TD_D0	U8.17	Video Decoder Data0 (Mode Control Register = 0 or 2)
60	HC_TD_D[1]	U4.M14	U4.T8	TD_D1	U8.16	Video Decoder Data1 (Mode Control Register = 0 or 2)

Table 2–23. Video Decoder Pinout with HSMC Connector

HSMC Connector		MAX II		Video Decoder		
Pin No.	Signal Name	HSMC Side	Device Side	Signal Name	Pin No.	Description
62	HC_TD_D[2]	U4.L14	U4.T9	TD_D2	U8.10	Video Decoder Data2 (Mode Control Register = 0 or 2)
66	HC_TD_D[3]	U4.L15	U4.V9	TD_D3	U8.9	Video Decoder Data3 (Mode Control Register = 0 or 2)
68	HC_TD_D[4]	U4.M12	U4.U9	TD_D4	U8.8	Video Decoder Data4 (Mode Control Register = 0 or 2)
72	HC_TD_D[5]	U4.L13	U4.U10	TD_D5	U8.7	Video Decoder Data5 (Mode Control Register = 0 or 2)
74	HC_TD_D[6]	U4.K15	U4.V10	TD_D6	U8.6	Video Decoder Data6 (Mode Control Register = 0 or 2)
78	HC_TD_D[7]	U4.K14	U4.T10	TD_D7	U8.5	Video Decoder Data7 (Mode Control Register = 0 or 2)
98	HC_TD_27MHZ	U4.G14	U4.U8	TD_27MHZ	U8.11	Video Decoder Clock Input
80	HC_TD_RESET	U4.J14	U4.U12	TD_RESET	U8.31	Video Decoder Reset
33	HC_I2C_SDAT	U10.1	U10.20	I2C_DATA	U8.33	I2C Data
34	HC_I2C_SCLK	U4.P15	U4.U11	I2C_SCLK	U8.34	I2C Clock
84	HC_TD_VS	U4.J15	U4.V11	TD_VS	U8.37	Video Decoder V_SYNC (Mode Control Register = 0)
86	HC_TD_HS	U4.H13	U4.T11	TD_HS	U8.39	Video Decoder H_SYNC (Mode Control Register = 0)

Figure 2–18 shows the Video Decoder interface schematic.

Figure 2–18. Video Decoder Interface Schematic



NTSC PAL Video Decoder Circuit

Uses the ADV7180 Multi-format SDTV Video Decoder

- Supports worldwide NTSC/PAL/SECAM color demodulation
- One 10-bit ADC, 4X over-sampling for CVBS
- Supports Composite Video (CVBS) RCA jack input
- Supports digital output formats: 8-bit ITU-R BT.656 YCrCb 4:2:2
- output + HS, VS, and FIELD
- Applications: DVD recorders, LCD TV, Set-top boxes, Digital TV
- Portable video devices

VGA DAC Interface

The board includes an Analog Devices ADV7123 VGA DAC and 16-pin D-SUB connector for VGA output. Table 2–24 below lists VGA DAC Interface board reference and manufacturing information.

Table 2–24. VGA Output DAC

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
U9	240 MHz Triple 10-Bit High Speed Video DAC	Analog Devices	ADV7123	www.analog.com

The VGA DAC interface features:

- 240-MHz triple 10-bit high-speed video DAC
- 15-pin high-density D-sub connector

The VGA synchronization signals are provided directly from the Cyclone III FPGA, and the Analog Devices ADV7123 triple 10-bit high-speed video DAC is used to produce the analog data signals (red, green, and blue).

Figure 2–19 illustrates the basic timing requirements for each row (horizontal) that is displayed on a VGA monitor. An active-low pulse of specific duration (time) as shown in the figure is applied to the horizontal synchronization (hsync) input of the monitor, which signifies the end of one row of data and the start of the next. The data (RGB) inputs on the monitor must be off (driven to 0 V) for a time period called the back porch (b) after the hsync pulse occurs, which is followed by the display interval (c). During the data display interval, the RGB data drives each pixel in turn across the row being displayed. Finally, there is a time period called the front porch (d) where the RGB signals must again be off before the next hsync pulse can occur. The timing of the vertical synchronization (vsync) is the same as shown in Figure 2–19, except that a vsync pulse signifies the end of one frame and the start of the next, and the data refers to the set of rows in the frame (horizontal timing). Table 2–25 and Table 2–26 show, for different resolutions, the durations of time periods a, b, c, and d for both horizontal and vertical timing.

On the LCD Multimedia HSMC users still need to multiplex the VGA synchronization and RGB data to fit the VGA TDM block input timing as mentioned in Figure 2–9 and Figure 2–10. The timing protocol of the VGA TDM controller is similar to the LCD TDM controller. The input color data bus HC_VGA_DATA changes from 8-bit to 10-bit, and the VGA TDM controller uses the HC_VGA_HS to determine the position of the BLUE color sample.

Figure 2–19. V.G.A. Horizontal Timing Specification

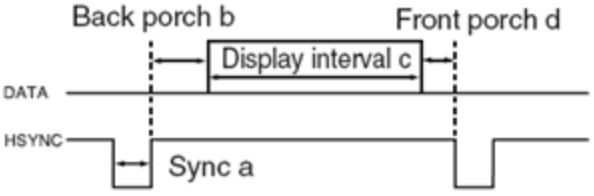


Table 2–25. VGA Horizontal Timing Specification

Configuration	Resolution(HxV)	a(us)	b(us)	c(us)	d(us)	Pixel clock(Mhz)
VGA(60Hz)	640x480	3.8	1.9	25.4	0.6	25 (640/c)
VGA(85Hz)	640x480	1.6	2.2	17.8	1.6	36 (640/c)
SVGA(60Hz)	800x600	3.2	2.2	20	1	40 (800/c)
SVGA(75Hz)	800x600	1.6	3.2	16.2	0.3	49 (800/c)
SVGA(85Hz)	800x600	1.1	2.7	14.2	0.6	56 (800/c)
XGA(60Hz)	1024x768	2.1	2.5	15.8	0.4	65 (1024/c)
XGA(70Hz)	1024x768	1.8	1.9	13.7	0.3	75 (1024/c)
XGA(85Hz)	1024x768	1.0	2.2	10.8	0.5	95 (1024/c)
1280x1024(60Hz)	1280x1024	1.0	2.3	11.9	0.4	108 (1280/c)

Table 2–26. VGA Vertical Timing Specification

Configuration	Resolution (HxV)	a(lines)	b(lines)	c(lines)	d(lines)
VGA(60Hz)	640x480	2	33	480	10
VGA(85Hz)	640x480	3	25	480	1
SVGA(60Hz)	800x600	4	23	600	1

Table 2–26. VGA Vertical Timing Specification

Configuration	Resolution (HxV)	a(lines)	b(lines)	c(lines)	d(lines)
SVGA(75Hz)	800x600	3	21	600	1
SVGA(85Hz)	800x600	3	27	600	1
XGA(60Hz)	1024x768	6	29	768	3
XGA(70Hz)	1024x768	6	29	768	3
XGA(85Hz)	1024x768	3	36	768	1
1280x1024(60Hz)	1280x1024	3	38	1024	1

Tables 2–27 shows the pinout of VGA/DAC Interface with HSMC connector.

Table 2–27. VGA/DAC Interface Pinout with HSMC Connector

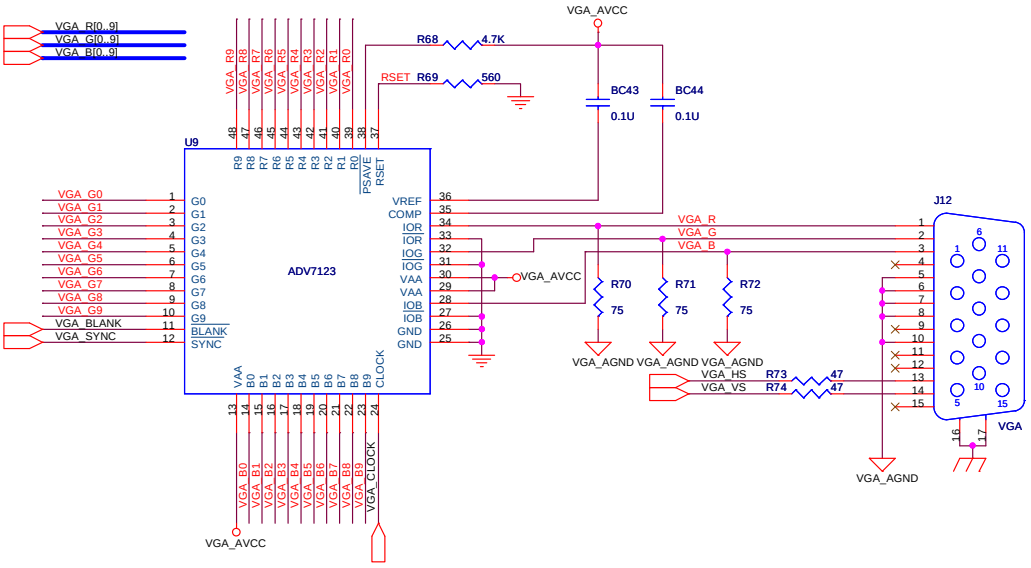
HSMC Connector		MAX II		VGA/DAC Interface		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_VGA_DATA[0]	65	N16	U7	VGA_R0	39	VGA red data bus bit 0
			V4	VGA_G0	1	VGA green data bus bit 0
			R7	VGA_B0	14	VGA blue data bus bit 0
HC_VGA_DATA[1]	67	M16	V7	VGA_R1	40	VGA red data bus bit 1
			U4	VGA_G1	2	VGA green data bus bit 1
			P6	VGA_B1	15	VGA blue data bus bit 1
HC_VGA_DATA[2]	71	M18	T7	VGA_R2	41	VGA red data bus bit 2
			U3	VGA_G2	3	VGA green data bus bit 2
			R6	VGA_B2	16	VGA blue data bus bit 2
HC_VGA_DATA[3]	73	M17	T6	VGA_R3	42	VGA red data bus bit 3
			V2	VGA_G3	4	VGA green data bus bit 3
			R5	VGA_B3	17	VGA blue data bus bit 3
HC_VGA_DATA[4]	77	L17	V6	VGA_R4	43	VGA red data bus bit 4
			P8	VGA_G4	5	VGA green data bus bit 4
			N4	VGA_B4	18	VGA blue data bus bit 4
HC_VGA_DATA[5]	79	L18	U6	VGA_R5	44	VGA red data bus bit 5
			R9	VGA_G5	6	VGA green data bus bit 5
			N5	VGA_B5	19	VGA blue data bus bit 5

Table 2–27. VGA/DAC Interface Pinout with HSMC Connector

HSMC Connector		MAX II		VGA/DAC Interface		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_VGA_DATA[6]	83	L16	U5	VGA_R6	45	VGA red data bus bit 6
			P9	VGA_G6	7	VGA green data bus bit 6
			M5	VGA_B6	20	VGA blue data bus bit 6
HC_VGA_DATA[7]	85	K16	V5	VGA_R7	46	VGA red data bus bit 7
			P10	VGA_G7	8	VGA green data bus bit 7
			M4	VGA_B7	21	VGA blue data bus bit 7
HC_VGA_DATA[8]	89	K18	T5	VGA_R8	47	VGA red data bus bit 8
			R10	VGA_G8	9	VGA green data bus bit 8
			M6	VGA_B8	22	VGA blue data bus bit 8
HC_VGA_DATA[9]	91	J18	T4	VGA_R9	48	VGA red data bus bit 9
			P11	VGA_G9	10	VGA green data bus bit 9
			L6	VGA_B9	23	VGA blue data bus bit 9
HC_VGA_BLANK	59	N17	R8	VGA_BLANK	11	VGA BLANK
HC_VGA_SYNC	61	N18	P7	VGA_SYNC	12	VGA SYNC
HC_VGA_CLOCK	97	J13	L4	VGA_CLOCK	24	VGA TDM Clock

Figure 2–20 shows the VGA/DAC interface schematic.

Figure 2–20. VGA/DAC Interface Schematic



Clocking Circuitry

The board has a number of dedicated clock oscillators that are used for system timing or timing of specific peripheral chips. A list of these oscillators is shown in Table 2–28 below.

Table 2–28. Oscillators

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
Y1	25MHz, 25ppm, CL=15pF, 3.3V, Size:5*7*1.4 mm	Mercury Electronics	FH3SWO-AT-25.000	www.mecxtal.com
Y2	100MHz, 25ppm, CL=15pF, 3.3V, Size:5*7*1.4 mm	Mercury Electronics	FH3SWO-AT-100.000	www.mecxtal.com
Y3	28MHz, 25ppm, CL=15pF, 3.3V, Size:5*7*1.4 mm	Mercury Electronics	FH3SWO-AT-27.000	www.mecxtal.com

Power Supply

Power Supplies

The power supply block distributes clean power from the 12 V and 3.3 V input supply (from HSMC connector) to the LCD Multimedia HSMC through on-board regulators. To provide various voltage options, the board uses several Linear Technologies' regulators. Switching regulators are used for digital circuits and linear regulators are used for analog circuits.

Table 2–29 below lists Power Supplies board reference and manufacturing information.

Table 2–29. Power Supplies Manufacturing Information

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
REG1	DC/DC Converter +/- 5V for LCD Display	Linear Technology	LT3461ES6#TRPBF	www.linear.com
REG2	DC/DC Converter for +/- Voltages for LCD Display Backlight	Linear Technology	LT3461ES6#TRPBF	www.linear.com
REG3	Linear regulator for 5V output	Linear Technology	LT1117CTS-5#PBF	www.linear.com
REG4	Linear regulator for 2.5V output	Linear Technology	LT1963AES8#PBF	www.linear.com
REG5	Linear regulator for 1.8V output	Linear Technology	LT1963AES8#PBF	www.linear.com

Board regulators are used to generate the voltages listed in Tables 2–30

Table 2–30. Board Regulators

Output Voltage (V)	Variance (+/-mV)	MAX Current (A)	Regulator Board Reference	Linear Technologies Part #	Where Used
5V	50 mV	115mA	REG1	LT3461ES6#TRPBF	LCD Supply
26.4V	100mV	-	REG2	LT3461ES6#TRPBF	LED Backlight
5V	50mV	800mA	REG3	LT1117CTS-5#PBF	PS2 Interface Supply
2.5V	27mV	1.5A	REG4	LT1963AES8#PBF	CPLD Bank Supply, Level Shifter Supply
1.8V	27mV	1.5A	REG5	LT1963AES8#PBF	Video Decoder Supply

EEPROM

I2C Serial EEPROM

There is a 2K-bits I2C Serial EEPROM on the LCD Multimedia HSMC that contains information used by applications for this board. Table 2–31 below lists I2C Serial EEPROM board reference and manufacturing information. This data can be read or written to the LCD Multimedia HSMC using the EEPROM and Mode switch utility as described in Appendix C.

Table 2–31. I2C Serial EEPROM Manufacturing Information

Board Reference	Device Description	Manufacturer	Manufacturer Part Number	Manufacturer Website
U3	2K-bits I2C Serial EEPROM	Microchip	24LC02B	www.microchip.com

Table 2–32 contains the data format written in the first 16 bytes of this EEPROM.

Table 2–32. EEPROM Data Format

Byte #s	Bit #s	Description	Value for LCD Multimedia HSMC
0	0-7	Number of bytes written (including Byte 0)	0x10
1(1)	0-3	Minor revision number	0x0
	4-7	Major revision number	0x2
2-7	0-7	Board Serial Number (If bytes 2-4 is “00 07 ED” then this is a MAC address.)	Altera MAC Addresses are in the format “00 07 ED 08 xx xx”. The "08" is the group for the LCD Multimedia HSMC. The last two bytes are sequential and incremented for each board.
8-15	0-7	8 bytes of board specific calibration data.	Calibration Data for TouchScreen is currently in the form of Upper Right X (3946 = 0x0f6a), Upper Right Y (3849 = 0x0f09), Lower Left X (132 = 0x0084), Lower Left Y (148 = 0x0094)

Notes:
(1) Version Number in the form of <Major>.<Minor>.

To provide better accuracy for the touch-screen portion of the LCD module, static calibration data has been programmed in bytes 8-15 of the EEPROM. This data is shown in Table 2–33.

Table 2–33. Byte values for touch screen calibration data

Byte	8	9	10	11	12	13	14	15
Value	0f	6a	0f	09	00	84	00	94
Coordinate	x=799		y=0		x=0		y=479	
Position	Upper Right				Lower Left			

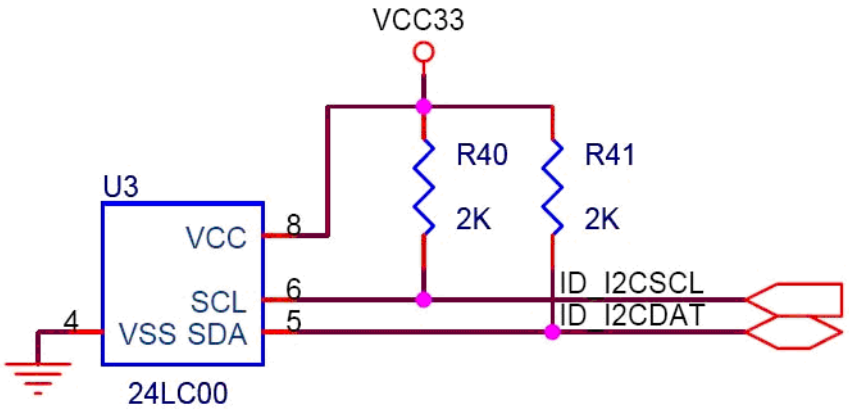
Table 2–34 shows the pinout of I2C Serial EEPROM with HSMC connector.

Table 2–34. I2C Serial EEPROM Pinout with HSMC Connector

I2C Serial EEPROM		MAX II		I2C Serial EEPROM		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_ID_I2CSCL	41	T17	N3	ID_I2CSCL	6	EEPROM I2C Clock
HC_ID_I2CDAT	42	P18	P3	ID_I2CDAT	5	EEPROM I2C Data

Figure 2–21 shows the I2C Serial EEPROM schematic.

Figure 2–21. I2C Serial EEPROM Schematic



Expansion Interface

HSMC Interface

The LCD Multimedia HSMC connects to Altera FPGA Starter and Development Boards via a single High Speed Mezzanine Card (HSMC) connector (J6).

Table 2–35 below lists HSMC A connector board reference and manufacturing information.

Table 2–35. HSMC A Connector Manufacturing Information

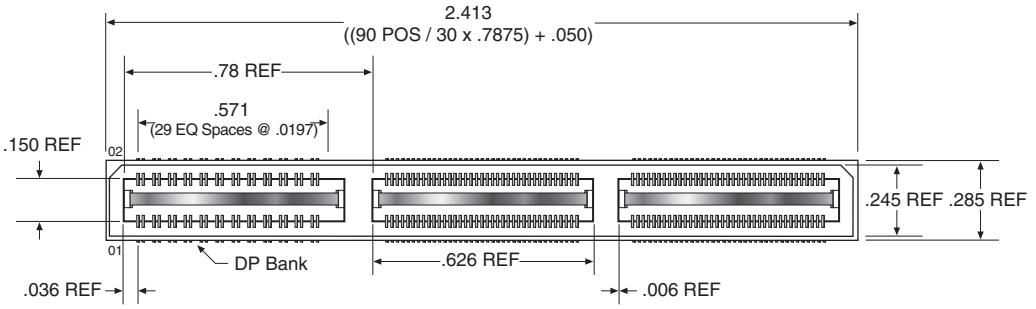
Board Reference	Description	Manufacturer	Manufacturer Part Number
J6	High Speed Mezzanine Card Connector	Samtec	ASP-122952-01

The HSMC connector is a modified version of standard high-speed Samtec connectors. To provide better integrity between host boards and HSMC boards when using high-speed transceivers, the standard high-speed Samtec connector is modified by removing every third pin in bank 1.

CMOS utilization of the HSMC pins is assumed and no options for supporting other differential signaling are provided with the board. The eight clock-data-recovery high-speed transceiver channels are not connected on this HSMC.

The HSMC connector layout is shown in Figures 2–22 below.

Figure 2–22. Samtec Header Connector



HSMC connector pinout information is shown throughout this document for each individual interface and in the appendices for connecting to various FPGA starter and development boards.

Statement of China-RoHS Compliance

Table 2–36 lists hazardous substances included with the kit.

Table 2–36. Table of Hazardous Substances' Name and Concentration, *Notes (1),(2)*

Part Name	Lead (Pb)	Cadmium (Cd)	Hexavalent Chromium (Cr6+)	Mercury (Hg)	Polybrominated biphenyls (PBB)	Polybrominated diphenyl Ethers (PBDE)
Cyclone III FPGA starter board	X*	0	0	0	0	0
12 V power supply	0	0	0	0	0	0
Type A-B USB cable	0	0	0	0	0	0
User guide	0	0	0	0	0	0

Notes to Table 2–36:

(1) 0 indicates that the concentration of the hazardous substance in all homogeneous materials in the parts is below the relevant threshold of the SJ/T11363-2006 standard.

(2) X* indicates that the concentration of the hazardous substance of at least one of all homogeneous materials in the parts is above the relevant threshold of the SJ/T11363-2006 standard, but it is exempted by EU RoHS.

Appendix A. Pinouts for the Cyclone III Starter Board

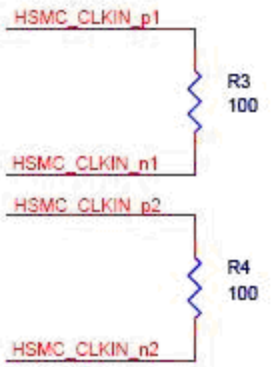
Introduction

The section describes the HSMC pin connections for Cyclone III Starter Board. See Tables A–2

Special caution when building applications with the LCD Multimedia HSMC and the Cyclone III FPGA Starter Board:

CAUTION

The LCD Multimedia HSMC uses the differential pair HSMC_CLKIN pins as single-ended I/O. On the Cyclone III Starter Board, the n and p signals for these pins are terminated with 100 Ohm resistors (R3 and R4).



These signals correspond to single-ended I/O on the LCD Multimedia HSMC. R3 connects HC_RX_CLK and HC_TD_27MHZ and R4 connects HC_ADC_PENIRQ_n and HC_TX_CLK. To avoid unwanted noise on signals, users are advised to turn off the peripherals as shown in the Table A–1 below.

The Cyclone III FPGA Starter Board schematic can be found at:<*installation directory*>/board_design_files/schematic/cycloneIII_3c25_start.

Table A–1. Settings to avoid unwanted noise across signals

When using this function	Disable this chip	Required Setting
Video Decoder	Ethernet PHY (U2)	Set **HC_ETH_RESET_N** to logic 0
Touch Panel	Ethernet PHY (U2)	Set **HC_ETH_RESET_N** to logic 0
Ethernet PHY	Video Decoder (U8)	Set **HC_TD_RESET** to logic 0 **Avoid** using touch-panel.

Table A–2. HSMC Interface Pinouts

LCD Multimedia HSMC v2.0 Schematic		Cyclone III Starter Board Schematic		Direction	Type
HSMC Pin #	Signal Name	Signal Name	FPGA Pin		
33	HC_I2C_SDAT	HSMC_SDA	E1	Bidirectional	2.5 V
34	HC_I2C_SCLK	HSMC_SCL	F3	Bidirectional	2.5 V
35	HSMC_TCK	HSMC_TCK	J1	-	-
36	HSMC_TMS	HSMC_TMS	J2	-	-
37	HSMC_TDO	HSMC_TDI	J6	-	-
38	HSMC_TDI	HSMC_TDO	J5	-	-
39	HC_AUD_XCK	HSMC_CLKOUT0	A1	Output	2.5 V
40	HC_AUD_ADCDAT	HSMC_CLKIN0	A9	Input	2.5 V
95	HC_ID_I2CSCL	HSMC_CLKOUT_p1	D14	Output	2.5 V
96	HC_ID_I2CDAT	HSMC_CLKIN_p1	F17	Input	2.5 V
97	HC_PS2_CLK	HSMC_CLKOUT_n1	C14	Output	2.5 V
98	HC_SD_CMD	HSMC_CLKIN_n1	F18	Input	2.5 V
155	HC_PS2_DAT	HSMC_CLKOUT_p2	U18	Output	2.5 V
156	HC_SD_DAT	HSMC_CLKIN_p2	N17	Input	2.5 V
157	HC_MDIO	HSMC_CLKOUT_n2	V18	Output	2.5 V
158	HC_SDA	HSMC_CLKIN_n2	N18	Input	2.5 V
41	HC_SD_DAT3	HSMC_D0	H6	Bidirectional	2.5 V
42	HC_VGA_HS	HSMC_D1	D3	Bidirectional	2.5 V

Table A–2. HSMC Interface Pinouts

LCD Multimedia HSMC v2.0 Schematic		Cyclone III Starter Board Schematic		Direction	Type
HSMC Pin #	Signal Name	Signal Name	FPGA Pin		
43	HC_VGA_VS	HSMC_D2	M5	Bidirectional	2.5 V
44	HC_TD_D0	HSMC_D3	L6	Bidirectional	2.5 V
47	HC_VGA_BLANK	HSMC_D4	T1	Bidirectional	2.5 V
48	HC_TD_D1	HSMC_D5	M3	Bidirectional	2.5 V
49	HC_VGA_SYNC	HSMC_D6	N7	Bidirectional	2.5 V
50	HC_TD_D2	HSMC_D7	T2	Bidirectional	2.5 V
53	HC_VGA_DATA0	HSMC_D8	N8	Bidirectional	2.5 V
54	HC_TD_D3	HSMC_D9	H15	Bidirectional	2.5 V
55	HC_VGA_DATA1	HSMC_D10	J13	Bidirectional	2.5 V
56	HC_TD_D4	HSMC_D11	H16	Bidirectional	2.5 V
59	HC_VGA_DATA2	HSMC_D12	N10	Bidirectional	2.5 V
60	HC_TD_D5	HSMC_D13	N16	Bidirectional	2.5 V
61	HC_VGA_DATA3	HSMC_D14	N11	Bidirectional	2.5 V
62	HC_TD_D6	HSMC_D15	N15	Bidirectional	2.5 V
65	HC_VGA_DATA4	HSMC_D16	K17	Bidirectional	2.5 V
66	HC_TD_D7	HSMC_D17	R16	Bidirectional	2.5 V
67	HC_VGA_DATA5	HSMC_D18	P11	Bidirectional	2.5 V
68	HC_TD_RESET	HSMC_D19	T16	Bidirectional	2.5 V
71	HC_VGA_DATA6	HSMC_TX_p4	B2	Bidirectional	2.5 V
72	HC_TD_VS	HSMC_RX_p4	C2	Bidirectional	2.5 V
73	HC_VGA_DATA7	HSMC_TX_n4	B1	Bidirectional	2.5 V
74	HC_TD_HS	HSMC_RX_n4	C1	Bidirectional	2.5 V
77	HC_VGA_DATA8	HSMC_TX_p5	G2	Bidirectional	2.5 V
78	HC_RX_ERR	HSMC_RX_p5	H2	Bidirectional	2.5 V
79	HC_VGA_DATA9	HSMC_TX_n5	G1	Bidirectional	2.5 V
80	HC_RX_CRS	HSMC_RX_n5	H1	Bidirectional	2.5 V
83	HC_NCLK	HSMC_TX_p6	K2	Bidirectional	2.5 V
84	HC_RX_CLK	HSMC_RX_p6	K5	Bidirectional	2.5 V
85	HC_VGA_CLOCK	HSMC_TX_n6	K1	Bidirectional	2.5 V
86	HC_TD_27MHZ	HSMC_RX_n6	L5	Bidirectional	2.5 V

Table A–2. HSMC Interface Pinouts

LCD Multimedia HSMC v2.0 Schematic		Cyclone III Starter Board Schematic		Direction	Type
HSMC Pin #	Signal Name	Signal Name	FPGA Pin		
89	HC_SD_CLK	HSMC_TX_p7	L2	Bidirectional	2.5 V
90	HC_RXD0	HSMC_RX_p7	L4	Bidirectional	2.5 V
91	HC_AUD_ADCLRCK	HSMC_TX_n7	L1	Bidirectional	2.5 V
92	HC_RXD1	HSMC_RX_n7	L3	Bidirectional	2.5 V
101	HC_AUD_DACLRCK	HSMC_TX_p8	M2	Bidirectional	2.5 V
102	HC_RXD2	HSMC_RX_p8	P2	Bidirectional	2.5 V
103	HC_AUD_DACDAT	HSMC_TX_n8	M1	Bidirectional	2.5 V
104	HC_RXD3	HSMC_RX_n8	P1	Bidirectional	2.5 V
107	HC_AUD_BCLK	HSMC_TX_p9	R2	Bidirectional	2.5 V
108	HC_RX_COL	HSMC_RX_p9	T3	Bidirectional	2.5 V
109	HC_UART_RXD	HSMC_TX_n9	R1	Bidirectional	2.5 V
110	HC_RX_DV	HSMC_RX_n9	R3	Bidirectional	2.5 V
113	HC_UART_TXD	HSMC_TX_p10	E17	Bidirectional	2.5 V
114	HC_ADC_BUSY	HSMC_RX_p10	G17	Bidirectional	2.5 V
115	HC_ETH_RESET_N	HSMC_TX_n10	E18	Bidirectional	2.5 V
116	HC_ADC_DOUT	HSMC_RX_n10	G18	Bidirectional	2.5 V
119	HC_TX_EN	HSMC_TX_p11	H17	Bidirectional	2.5 V
120	HC_LCD_DATA3	HSMC_RX_p11	K18	Bidirectional	2.5 V
121	HC_TXD0	HSMC_TX_n11	H18	Bidirectional	2.5 V
122	HC_LCD_DATA4	HSMC_RX_n11	L18	Bidirectional	2.5 V
125	HC_TXD1	HSMC_TX_p12	L17	Bidirectional	2.5 V
126	HC_VD	HSMC_RX_p12	L16	Bidirectional	2.5 V
127	HC_TXD2	HSMC_TX_n12	M18	Bidirectional	2.5 V
128	HC_HD	HSMC_RX_n12	M17	Bidirectional	2.5 V
131	HC_TXD3	HSMC_TX_p13	L14	Bidirectional	2.5 V
132	HC_DEN	HSMC_RX_p13	L13	Bidirectional	2.5 V
133	HC_MDC	HSMC_TX_n13	L15	Bidirectional	2.5 V
134	HC_GREST	HSMC_RX_n13	M14	Bidirectional	2.5 V
137	HC_ADC_CS_n	HSMC_TX_p14	P17	Bidirectional	2.5 V
138	HC_SCEN	HSMC_RX_p14	R17	Bidirectional	2.5 V

Table A–2. HSMC Interface Pinouts

LCD Multimedia HSMC v2.0 Schematic		Cyclone III Starter Board Schematic		Direction	Type
HSMC Pin #	Signal Name	Signal Name	FPGA Pin		
139	HC_LCD_DATA0	HSMC_TX_n14	P18	Bidirectional	2.5 V
140	HC_LCD_DATA5	HSMC_RX_n14	R18	Bidirectional	2.5 V
143	HC_LCD_DATA1	HSMC_TX_p15	R5	Bidirectional	2.5 V
144	HC_LCD_DATA6	HSMC_RX_p15	M6	Bidirectional	2.5 V
145	HC_LCD_DATA2	HSMC_TX_n15	R4	Bidirectional	2.5 V
146	HC_LCD_DATA7	HSMC_RX_n15	N6	Bidirectional	2.5 V
149	HC_ADC_DIN	HSMC_TX_p16	T17	Bidirectional	2.5 V
150	HC_ADC_PENIRQ_n	HSMC_RX_p16	M13	Bidirectional	2.5 V
151	HC_ADC_DCLK	HSMC_TX_n16	T18	Bidirectional	2.5 V
152	HC_TX_CLK	HSMC_RX_n16	N13	Bidirectional	2.5 V

Appendix B. Pinouts for the Cyclone III Development Board

Introduction

The section describes the pinouts for the HSMC Port A interface, Cyclone III Development Board. See Tables B–1

The Cyclone III FPGA Development Board schematic can be found at:<*installation directory*>/**board_design_files/cycloneIII_3c120_dev/schematic/**.

Table B–1. HSMC Port A (J8) Interface Pinouts

LCD Multimedia HSMC v2.0 Schematic		Cyclone III Development Board Schematic		Direction	Type
HSMC (J6) Pin #	HSMC Connector (J6) Signal Name	Signal Name	FPGA (U20) Pin No.		
33	HC_I2C_SDAT	HSMA_SDA	AC1	Bidirectional	2.5 V
34	HC_I2C_SCLK	HSMA_SCL	AC3	Bidirectional	2.5 V
35	HSMC_TCK	FPGA_JTAG_TCK	P5	-	-
36	HSMC_TMS	FPGA_JTAG_TMS	P8	-	-
37	HSMC_TDO	HSMA_JTAG_TDO	-	-	-
38	HSMC_TDI	HSMA_JTAG_TDI	-	-	-
39	HC_AUD_XCK	HSMA_CLK_OUT0	Y7	Output	2.5 V
40	HC_AUD_ADCDAT	HSMA_CLK_IN0	AG14	Input	2.5 V
41	HC_ID_I2CSCL	HSMA_D0	AB6	Output	2.5 V
42	HC_ID_I2CDAT	HSMA_D1	AF2	Input	2.5 V
43	HC_PS2_CLK	HSMA_D2	AE3	Output	2.5 V
44	HC_SD_CMD	HSMA_D3	AC5	Input	2.5 V
47	HC_PS2_DAT	HSMA_TX_D_P0	R7	Output	2.5 V
48	HC_SD_DAT	HSMA_RX_D_P0	AB2	Input	2.5 V
49	HC_MDIO	HSMA_TX_D_N0	R6	Output	2.5 V
50	HC_SDA	HSMA_RX_D_N0	AB1	Input	2.5 V
53	HC_SD_DAT3	HSMA_TX_D_P1	V4	Bidirectional	2.5 V
54	HC_VGA_HS	HSMA_RX_D_P1	Y4	Bidirectional	2.5 V
55	HC_VGA_VS	HSMA_TX_D_N1	V3	Bidirectional	2.5 V

Table B–1. HSMC Port A (J8) Interface Pinouts

LCD Multimedia HSMC v2.0 Schematic		Cyclone III Development Board Schematic		Direction	Type
HSMC (J6) Pin #	HSMC Connector (J6) Signal Name	Signal Name	FPGA (U20) Pin No.		
56	HC_TD_D0	HSMA_RX_D_N1	Y3	Bidirectional	2.5 V
59	HC_VGA_BLANK	HSMA_TX_D_P2	T4	Bidirectional	2.5 V
60	HC_TD_D1	HSMA_RX_D_P2	U3	Bidirectional	2.5 V
61	HC_VGA_SYNC	HSMA_TX_D_N2	T3	Bidirectional	2.5 V
62	HC_TD_D2	HSMA_RX_D_N2	U4	Bidirectional	2.5 V
65	HC_VGA_DATA0	HSMA_TX_D_P3	R3	Bidirectional	2.5 V
66	HC_TD_D3	HSMA_RX_D_P3	W2	Bidirectional	2.5 V
67	HC_VGA_DATA1	HSMA_TX_D_N3	R4	Bidirectional	2.5 V
68	HC_TD_D4	HSMA_RX_D_N3	W1	Bidirectional	2.5 V
71	HC_VGA_DATA2	HSMA_TX_D_P4	M8	Bidirectional	2.5 V
72	HC_TD_D5	HSMA_RX_D_P4	V2	Bidirectional	2.5 V
73	HC_VGA_DATA3	HSMA_TX_D_N4	M7	Bidirectional	2.5 V
74	HC_TD_D6	HSMA_RX_D_N4	V1	Bidirectional	2.5 V
77	HC_VGA_DATA4	HSMA_TX_D_P5	P2	Bidirectional	2.5 V
78	HC_TD_D7	HSMA_RX_D_P5	U2	Bidirectional	2.5 V
79	HC_VGA_DATA5	HSMA_TX_D_N5	P1	Bidirectional	2.5 V
80	HC_TD_RESET	HSMA_RX_D_N5	U1	Bidirectional	2.5 V
83	HC_VGA_DATA6	HSMA_TX_D_P6	M4	Bidirectional	2.5 V
84	HC_TD_VS	HSMA_RX_D_P6	U6	Bidirectional	2.5 V
85	HC_VGA_DATA7	HSMA_TX_D_N6	M3	Bidirectional	2.5 V
86	HC_TD_HS	HSMA_RX_D_N6	U5	Bidirectional	2.5 V
89	HC_VGA_DATA8	HSMA_TX_D_P7	M2	Bidirectional	2.5 V
90	HC_RX_ERR	HSMA_RX_D_P7	R2	Bidirectional	2.5 V
91	HC_VGA_DATA9	HSMA_TX_D_N7	M1	Bidirectional	2.5 V
92	HC_RX_CRS	HSMA_RX_D_N7	R1	Bidirectional	2.5 V
95	HC_NCLK	HSMA_CLK_OUT_P1	G6	Bidirectional	2.5 V
96	HC_RX_CLK	HSMA_CLK_IN_P1	Y2	Bidirectional	2.5 V
97	HC_VGA_CLOCK	HSMA_CLK_OUT_N1	G5	Bidirectional	2.5 V
98	HC_TD_27MHZ	HSMA_CLK_IN_N1	Y1	Bidirectional	2.5 V

Table B–1. HSMC Port A (J8) Interface Pinouts

LCD Multimedia HSMC v2.0 Schematic		Cyclone III Development Board Schematic		Direction	Type
HSMC (J6) Pin #	HSMC Connector (J6) Signal Name	Signal Name	FPGA (U20) Pin No.		
101	HC_SD_CLK	HSMA_TX_D_P8	L7	Bidirectional	2.5 V
102	HC_RXD0	HSMA_RX_D_P8	N4	Bidirectional	2.5 V
103	HC_AUD_ADCLRCK	HSMA_TX_D_N8	L6	Bidirectional	2.5 V
104	HC_RXD1	HSMA_RX_D_N8	N3	Bidirectional	2.5 V
107	HC_AUD_DACLRCK	HSMA_TX_D_P9	K8	Bidirectional	2.5 V
108	HC_RXD2	HSMA_RX_D_P9	L4	Bidirectional	2.5 V
109	HC_AUD_DACDAT	HSMA_TX_D_N9	L8	Bidirectional	2.5 V
110	HC_RXD3	HSMA_RX_D_N9	L3	Bidirectional	2.5 V
113	HC_AUD_BCLK	HSMA_TX_D_P10	K4	Bidirectional	2.5 V
114	HC_RX_COL	HSMA_RX_D_P10	L2	Bidirectional	2.5 V
115	HC_UART_RXD	HSMA_TX_D_N10	K3	Bidirectional	2.5 V
116	HC_RX_DV	HSMA_RX_D_N10	L1	Bidirectional	2.5 V
119	HC_UART_TXD	HSMA_TX_D_P11	J4	Bidirectional	2.5 V
120	HC_ADC_BUSY	HSMA_RX_D_P11	K2	Bidirectional	2.5 V
121	HC_ETH_RESET_N	HSMA_TX_D_N11	J3	Bidirectional	2.5 V
122	HC_ADC_DOUT	HSMA_RX_D_N11	K1	Bidirectional	2.5 V
125	HC_TX_EN	HSMA_TX_D_P12	J7	Bidirectional	2.5 V
126	HC_LCD_DATA3	HSMA_RX_D_P12	J6	Bidirectional	2.5 V
127	HC_TXD0	HSMA_TX_D_N12	K7	Bidirectional	2.5 V
128	HC_LCD_DATA4	HSMA_RX_D_N12	J5	Bidirectional	2.5 V
131	HC_TXD1	HSMA_TX_D_P13	G2	Bidirectional	2.5 V
132	HC_VD	HSMA_RX_D_P13	H4	Bidirectional	2.5 V
133	HC_TXD2	HSMA_TX_D_N13	G1	Bidirectional	2.5 V
134	HC_HD	HSMA_RX_D_N13	H3	Bidirectional	2.5 V
137	HC_TXD3	HSMA_TX_D_P14	F5	Bidirectional	2.5 V
138	HC_DEN	HSMA_RX_D_P14	G4	Bidirectional	2.5 V
139	HC_MDC	HSMA_TX_D_N14	F4	Bidirectional	2.5 V
140	HC_GREST	HSMA_RX_D_N14	G3	Bidirectional	2.5 V
143	HC_ADC_CS_n	HSMA_TX_D_P15	E2	Bidirectional	2.5 V

Table B–1. HSMC Port A (J8) Interface Pinouts

LCD Multimedia HSMC v2.0 Schematic		Cyclone III Development Board Schematic		Direction	Type
HSMC (J6) Pin #	HSMC Connector (J6) Signal Name	Signal Name	FPGA (U20) Pin No.		
144	HC_SCEN	HSMA_RX_D_P15	F2	Bidirectional	2.5 V
145	HC_LCD_DATA0	HSMA_TX_D_N15	E1	Bidirectional	2.5 V
146	HC_LCD_DATA5	HSMA_RX_D_N15	F1	Bidirectional	2.5 V
149	HC_LCD_DATA1	HSMA_TX_D_P16	D3	Bidirectional	2.5 V
150	HC_LCD_DATA6	HSMA_RX_D_P16	E3	Bidirectional	2.5 V
151	HC_LCD_DATA2	HSMA_TX_D_N16	C2	Bidirectional	2.5 V
152	HC_LCD_DATA7	HSMA_RX_D_N16	F3	Bidirectional	2.5 V
155	HC_ADC_DIN	HSMA_CLK_OUT_P2	D2	Bidirectional	2.5 V
156	HC_ADC_PENIRQ_n	HSMA_CLK_IN_P2	J2	Bidirectional	2.5 V
157	HC_ADC_DCLK	HSMA_CLK_OUT_N2	D1	Bidirectional	2.5 V
158	HC_TX_CLK	HSMA_CLK_IN_N2	J1	Bidirectional	2.5 V

The section describes the pinouts for the HSMC Port B interface, Cyclone III Development Board. See Tables B–2

Table B–2. HSMC Port B (J9) Interface Pinouts

LCD Multimedia HSMC v2.0 Schematic		Cyclone III Development Board Schematic		Direction	Type
HSMC (J6) Pin #	HSMC (J6) Signal Name	Signal Name	FPGA (U20) Pin #		
33	HC_I2C_SDAT	HSMB_SDA	H26	Bidirectional	2.5 V
34	HC_I2C_SCLK	HSMB_SCL	H25	Bidirectional	2.5 V
35	HSMC_TCK	FPGA_JTAG_TCK	P5	-	-
36	HSMC_TMS	FPGA_JTAG_TMS	P8	-	-
37	HSMC_TDO	HSMB_JTAG_TDO	-	-	-
38	HSMC_TDI	HSMB_JTAG_TDI	-	-	-
39	HC_AUD_XCK	HSMB_CLK_OUT0	J22	Output	2.5 V
40	HC_AUD_ADCDAT	HSMB_CLK_IN0	A15	Input	2.5 V
41	HC_ID_I2CSCL	HSMB_D0	G24	Output	2.5 V

Table B–2. HSMC Port B (J9) Interface Pinouts

LCD Multimedia HSMC v2.0 Schematic		Cyclone III Development Board Schematic		Direction	Type
HSMC (J6) Pin #	HSMC (J6) Signal Name	Signal Name	FPGA (U20) Pin #		
42	HC_ID_I2CDAT	HSMB_D1	H23	Input	2.5 V
43	HC_PS2_CLK	HSMB_D2	G25	Output	2.5 V
44	HC_SD_CMD	HSMB_D3	H24	Input	2.5 V
47	HC_PS2_DAT	HSMB_TX_D_P0	J25	Output	2.5 V
48	HC_SD_DAT	HSMB_RX_D_P0	F27	Input	2.5 V
49	HC_MDIO	HSMB_TX_D_N0	J26	Output	2.5 V
50	HC_SDA	HSMB_RX_D_N0	F28	Input	2.5 V
53	HC_SD_DAT3	HSMB_TX_D_P1	L23	Bidirectional	2.5 V
54	HC_VGA_HS	HSMB_RX_D_P1	G27	Bidirectional	2.5 V
55	HC_VGA_VS	HSMB_TX_D_N1	L24	Bidirectional	2.5 V
56	HC_TD_D0	HSMB_RX_D_N1	G28	Bidirectional	2.5 V
59	HC_VGA_BLANK	HSMB_TX_D_P2	M25	Bidirectional	2.5 V
60	HC_TD_D1	HSMB_RX_D_P2	K25	Bidirectional	2.5 V
61	HC_VGA_SYNC	HSMB_TX_D_N2	M26	Bidirectional	2.5 V
62	HC_TD_D2	HSMB_RX_D_N2	K26	Bidirectional	2.5 V
65	HC_VGA_DATA0	HSMB_TX_D_P3	N25	Bidirectional	2.5 V
66	HC_TD_D3	HSMB_RX_D_P3	K27	Bidirectional	2.5 V
67	HC_VGA_DATA1	HSMB_TX_D_N3	N26	Bidirectional	2.5 V
68	HC_TD_D4	HSMB_RX_D_N3	K28	Bidirectional	2.5 V
71	HC_VGA_DATA2	HSMB_TX_D_P4	R27	Bidirectional	2.5 V
72	HC_TD_D5	HSMB_RX_D_P4	L27	Bidirectional	2.5 V
73	HC_VGA_DATA3	HSMB_TX_D_N4	R28	Bidirectional	2.5 V
74	HC_TD_D6	HSMB_RX_D_N4	L28	Bidirectional	2.5 V
77	HC_VGA_DATA4	HSMB_TX_D_P5	R25	Bidirectional	2.5 V
78	HC_TD_D7	HSMB_RX_D_P5	M27	Bidirectional	2.5 V
79	HC_VGA_DATA5	HSMB_TX_D_N5	R26	Bidirectional	2.5 V
80	HC_TD_RESET	HSMB_RX_D_N5	M28	Bidirectional	2.5 V
83	HC_VGA_DATA6	HSMB_TX_D_P6	U25	Bidirectional	2.5 V
84	HC_TD_VS	HSMB_RX_D_P6	P25	Bidirectional	2.5 V

Table B–2. HSMC Port B (J9) Interface Pinouts

LCD Multimedia HSMC v2.0 Schematic		Cyclone III Development Board Schematic		Direction	Type
HSMC (J6) Pin #	HSMC (J6) Signal Name	Signal Name	FPGA (U20) Pin #		
85	HC_VGA_DATA7	HSMB_TX_D_N6	U26	Bidirectional	2.5 V
86	HC_TD_HS	HSMB_RX_D_N6	P26	Bidirectional	2.5 V
89	HC_VGA_DATA8	HSMB_TX_D_P7	V27	Bidirectional	2.5 V
90	HC_RX_ERR	HSMB_RX_D_P7	P27	Bidirectional	2.5 V
91	HC_VGA_DATA9	HSMB_TX_D_N7	V28	Bidirectional	2.5 V
92	HC_RX_CRS	HSMB_RX_D_N7	P28	Bidirectional	2.5 V
95	HC_NCLK	HSMB_CLK_OUT_P1	AC26	Bidirectional	2.5 V
96	HC_RX_CLK	HSMB_CLK_IN_P1	J27	Bidirectional	2.5 V
97	HC_VGA_CLOCK	HSMB_CLK_OUT_N1	AD26	Bidirectional	2.5 V
98	HC_TD_27MHZ	HSMB_CLK_IN_N1	J28	Bidirectional	2.5 V
101	HC_SD_CLK	HSMB_TX_D_P8	V25	Bidirectional	2.5 V
102	HC_RXD0	HSMB_RX_D_P8	P21	Bidirectional	2.5 V
103	HC_AUD_ADCLRCK	HSMB_TX_D_N8	V26	Bidirectional	2.5 V
104	HC_RXD1	HSMB_RX_D_N8	R21	Bidirectional	2.5 V
107	HC_AUD_DACLRCK	HSMB_TX_D_P9	W25	Bidirectional	2.5 V
108	HC_RXD2	HSMB_RX_D_P9	R22	Bidirectional	2.5 V
109	HC_AUD_DACDAT	HSMB_TX_D_N9	W26	Bidirectional	2.5 V
110	HC_RXD3	HSMB_RX_D_N9	R23	Bidirectional	2.5 V
113	HC_AUD_BCLK	HSMB_TX_D_P10	Y25	Bidirectional	2.5 V
114	HC_RX_COL	HSMB_RX_D_P10	T25	Bidirectional	2.5 V
115	HC_UART_RXD	HSMB_TX_D_N10	Y26	Bidirectional	2.5 V
116	HC_RX_DV	HSMB_RX_D_N10	T26	Bidirectional	2.5 V
119	HC_UART_TXD	HSMB_TX_D_P11	AA25	Bidirectional	2.5 V
120	HC_ADC_BUSY	HSMB_RX_D_P11	U27	Bidirectional	2.5 V
121	HC_ETH_RESET_N	HSMB_TX_D_N11	AA26	Bidirectional	2.5 V
122	HC_ADC_DOUT	HSMB_RX_D_N11	U28	Bidirectional	2.5 V
125	HC_TX_EN	HSMB_TX_D_P12	AB25	Bidirectional	2.5 V
126	HC_LCD_DATA3	HSMB_RX_D_P12	U22	Bidirectional	2.5 V
127	HC_TXD0	HSMB_TX_D_N12	AB26	Bidirectional	2.5 V

Table B–2. HSMC Port B (J9) Interface Pinouts

LCD Multimedia HSMC v2.0 Schematic		Cyclone III Development Board Schematic		Direction	Type
HSMC (J6) Pin #	HSMC (J6) Signal Name	Signal Name	FPGA (U20) Pin #		
128	HC_LCD_DATA4	HSMB_RX_D_N12	V22	Bidirectional	2.5 V
131	HC_TXD1	HSMB_TX_D_P13	Y23	Bidirectional	2.5 V
132	HC_VD	HSMB_RX_D_P13	W28	Bidirectional	2.5 V
133	HC_TXD2	HSMB_TX_D_N13	Y24	Bidirectional	2.5 V
134	HC_HD	HSMB_RX_D_N13	W27	Bidirectional	2.5 V
137	HC_TXD3	HSMB_TX_D_P14	AE27	Bidirectional	2.5 V
138	HC_DEN	HSMB_RX_D_P14	V23	Bidirectional	2.5 V
139	HC_MDC	HSMB_TX_D_N14	AE28	Bidirectional	2.5 V
140	HC_GREST	HSMB_RX_D_N14	V24	Bidirectional	2.5 V
143	HC_ADC_CS_n	HSMB_TX_D_P15	W22	Bidirectional	2.5 V
144	HC_SCEN	HSMB_RX_D_P15	AB27	Bidirectional	2.5 V
145	HC_LCD_DATA0	HSMB_TX_D_N15	Y22	Bidirectional	2.5 V
146	HC_LCD_DATA5	HSMB_RX_D_N15	AB28	Bidirectional	2.5 V
149	HC_LCD_DATA1	HSMB_TX_D_P16	V21	Bidirectional	2.5 V
150	HC_LCD_DATA6	HSMB_RX_D_P16	AC27	Bidirectional	2.5 V
151	HC_LCD_DATA2	HSMB_TX_D_N16	W21	Bidirectional	2.5 V
152	HC_LCD_DATA7	HSMB_RX_D_N16	AC28	Bidirectional	2.5 V
155	HC_ADC_DIN	HSMB_CLK_OUT_P2	AD27	Bidirectional	2.5 V
156	HC_ADC_PENIRQ_n	HSMB_CLK_IN_P2	Y27	Bidirectional	2.5 V
157	HC_ADC_DCLK	HSMB_CLK_OUT_N2	AD28	Bidirectional	2.5 V
158	HC_TX_CLK	HSMB_CLK_IN_N2	Y28	Bidirectional	2.5 V

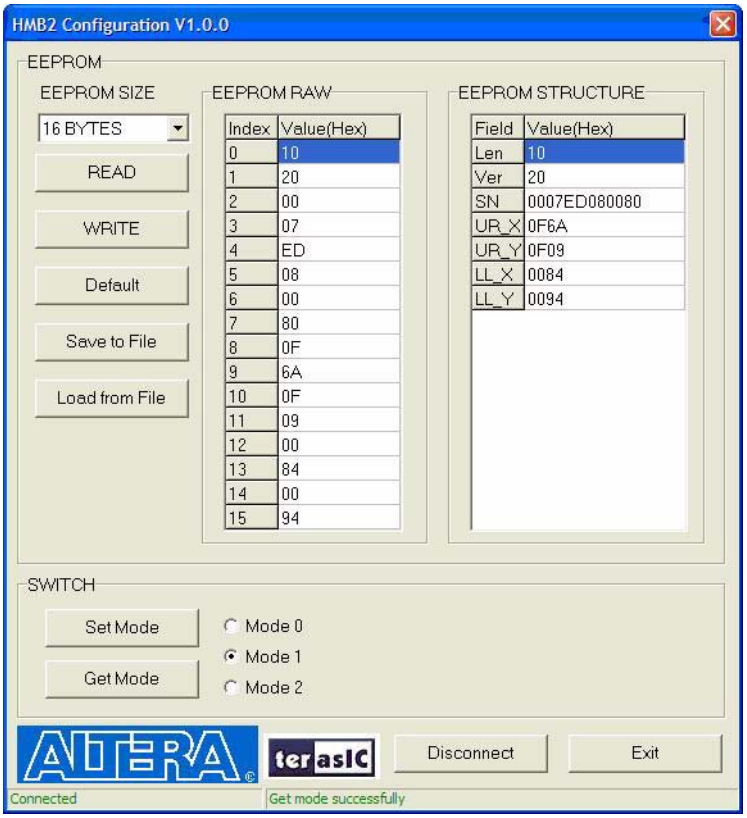
Appendix C. EEPROM and Mode Switch Utility

A common utility application is provided that allows you to change the EEPROM data or the Mode Control Register value stored in the MAX II Device's user flash memory. This appendix describes how to use this utility.

Starting the EEPROM and Mode Switch Utility (HMB2_CONFIG.exe)

1. Before using this tool, make sure the USB cable is connected to between the development kit board and the host PC.
2. From the directory: *<install dir>*/**board_design_files/LCD_multimedia_hsmc/tools/HMB2_Configuration_Utility,** launch **HMB2_CONFIG.exe**. (Figure C–1 shows the switch tool as it is launched).
3. There should be a .sof file in this directory (**HMB2_CONFIG.sof**) that will automatically download into the FPGA and the application will display **Connected** when communications is established with the downloaded design. (If any error message is shown, please check the power and USB cable, then press **Connect** button to re-configure FPGA.)

Figure C–1. EEPROM Switch Utility



Changing the contents of the EEPROM device

4. Using the buttons to the left of the **EEPROM** section of this utility you can:

   a. **READ:** Read the current contents of the EEPROM

   b. **WRITE:** Write the values shown in the EEPROM RAW section

   c. **Default:** Reset the valued in the EEPROM RAW section to a default set of values.

   d. **Save to File:** Save the data read from the EEPROM to a file.

   e. **Load from File:** Load values into the EEPROM RAW section.

Changing the Mode Control Register Setting in the MAX II device

5. By clicking on **Get Mode** button, the value currently stored in the mode-control register will be displayed.

6. To change the mode, select a different Mode Control Register value and then click the **Set Mode** button.

Refer back to Table 2–7 in the section "Bidirectional level shift interfaces and the Mode Control Registers" for an explanation of each of these modes.

Additional Information

Revision History

The table below displays the revision history for the chapters of the kit.

Chapter	Date	Version	Changes Made
All	December 2008	1.0.2	• Added LCD Multimedia HSMC Side View2 (Version 2.0) picture. • Added General purpose IO Connector (Mode 1 and 2 only) section. • Added Level Translators and MAX II Mode Control Register section. • Updated SD Card section • Added Appendix C.
All	August 2008	1.0.1	• Replaced LCD Multimedia Daughtercard with LCD Multimedia HSMC. • Modified Warning in Appendix-A. • Modified Document Part No.
All	November 2007	1.0.0	• First publication.

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Technical support	www.altera.com/mysupport/
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Product literature services	literature@altera.com
FTP site	ftp.altera.com

Note to table:
(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.*
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>***.pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input.` Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● •	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
	The hand points to information that requires special attention.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or the user's work.
	A warning calls attention to a condition or possible situation that can cause injury to the user.
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.