UNIVERSITY OF NEBRASKA-LINCOLN
Department of Electrical and Computer Engineering

ECEN-370 Digital Logic Design Fall, 2018

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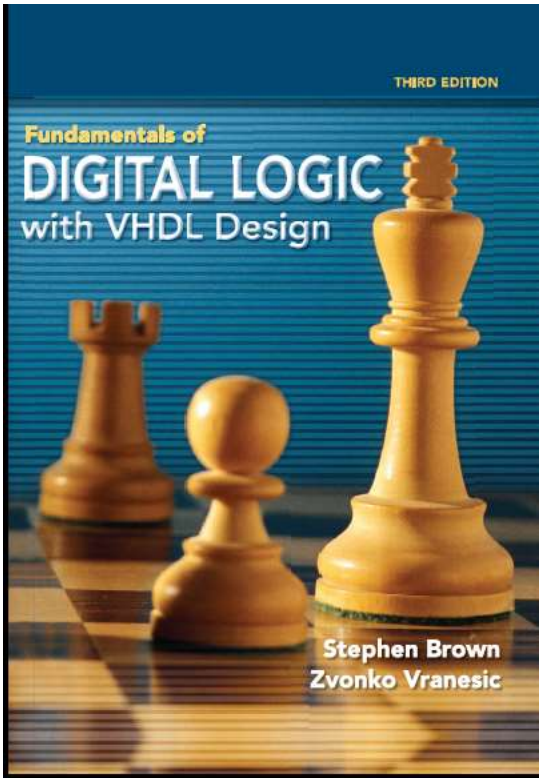
Textbook: Fundamentals of Digital Logic with VHDL Design, Third Edition
by Stephen Brown and Zvonko Vranesic, McGraw Hill



Lab Kit: **Intel/Altera Terasic DE10- Lite**

Prerequisite ELEC 122 or CSCE 230
Cross-listed CSCE 335

Goal:

1. Combine logic gates into a functional representation
2. Know implementation technology using PMOS, NMOS, and CMOS circuits
3. Minimize single and multiple output combinational logic circuits
4. Design combinational circuits using medium scale integrated (MSI) components.
5. Analyze and design synchronous sequential circuits
6. Be familiar with designs using FPGAs
7. Be familiar with using a hardware description language

Prerequisite

1. Demonstrate working familiarity with binary numbers and number systems including sign-magnitude, one's complement, and two's complement;
   (Review section 1.6, pp. 18-20 of the text)
2. Know the function of logic gates and combine them into a functional representation (e.g., minterms, maxterms, and truth tables), Chapter #2, Sections 2.1- 2.4, PP. 22- 31;
3. Simplify Boolean expressions using Karnaugh maps and implement them using 2-level all NAND and 2-level all NOR gates; Chapter #2, Sections 2.7- pp.47-51 and Chapter #4, Sections 4.1, PP. 168-175
4. Know registers and counters, Chapter #7, Sections 7.8-7.9; pp. 401- 411

Course Contents:

Chapter 2: Introduction to Logic Circuits (Sections 2.5, 2.8)
Chapter 3: Implementation Technology (Sections 3.1-3.10)
Chapter 4: Optimization of Boolean functions (Sections 4.2-4.7, 4.9)
Quine-McCluskey's method for single and multi-output functions
Chapter 5: Representation of Real Numbers and Arithmetic Circuits (Sections 5.2-5.4, 5.7)
Chapter 6: Combinational-Circuit Building Blocks (Sections 6.1-6.6)
Chapter 7: Flip-Flops, Registers, Counters (7.1-7.8, 7.11, 7.15)
Chapter 8: Synchronous Sequential Circuits (8.1- 8.12)
Chapter 9: Asynchronous Sequential Circuits (if time permits) (Sections 9.1-9.7)